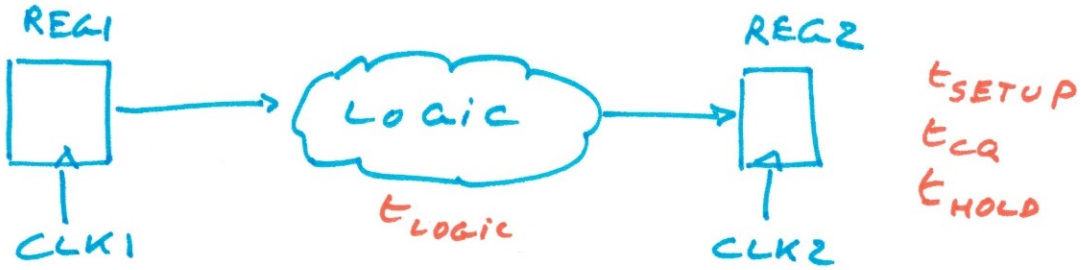
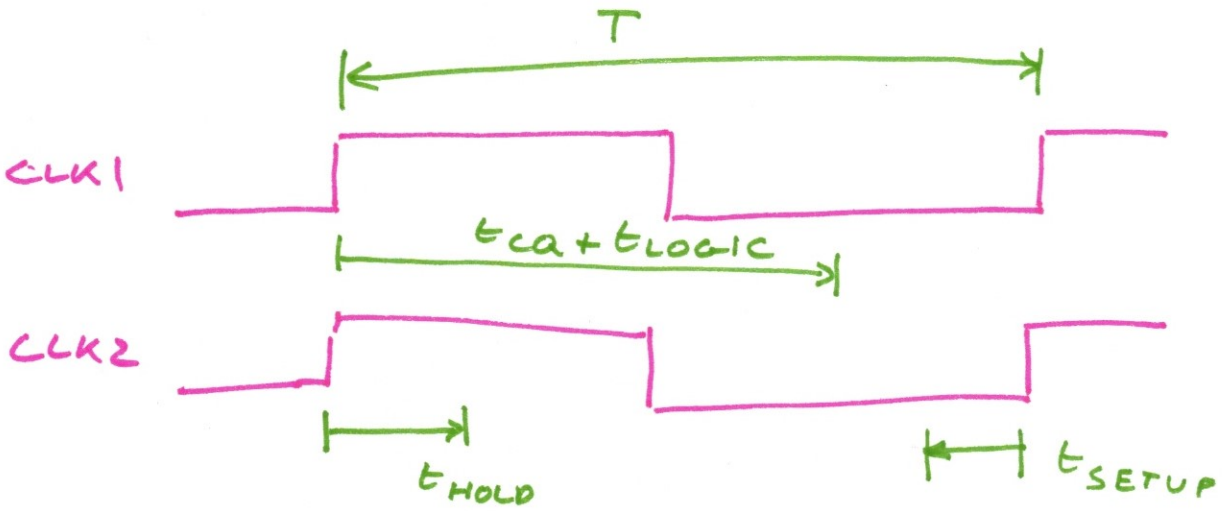
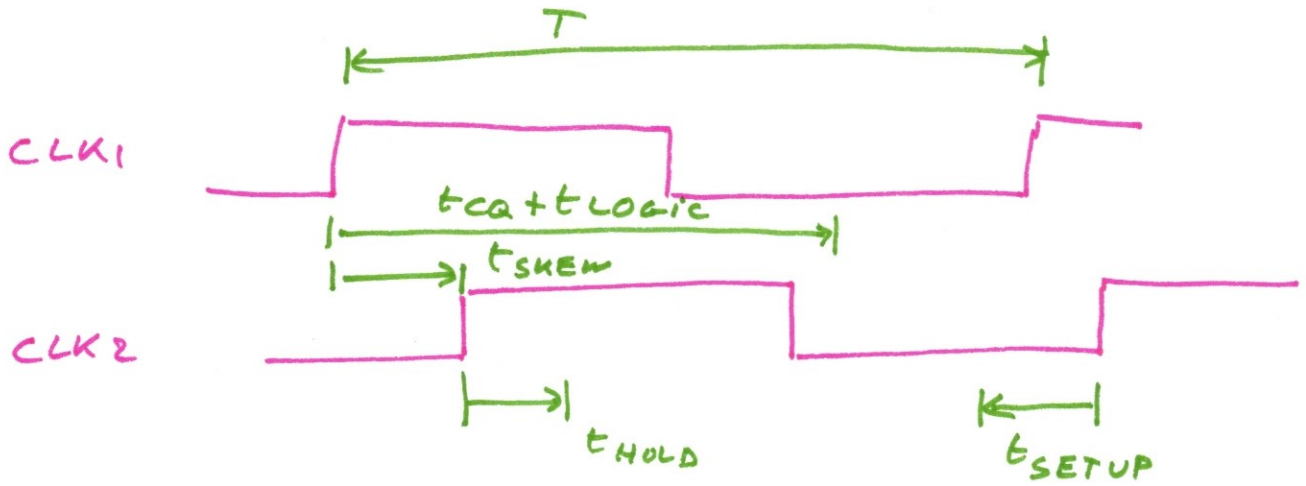
DESIGN WITH MULTIPLE CLOCKS





① $T > t_{CQ} + t_{LOGIC} + t_{SETUP}$

② $t_{HOLD} < t_{CQ} + t_{LOGIC}$

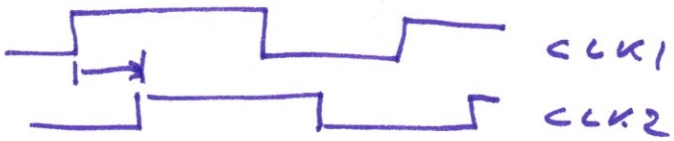


(1) $T + t_{SKEW} > t_{CQ} + t_{Logic} + t_{SETUP}$ GOOD!

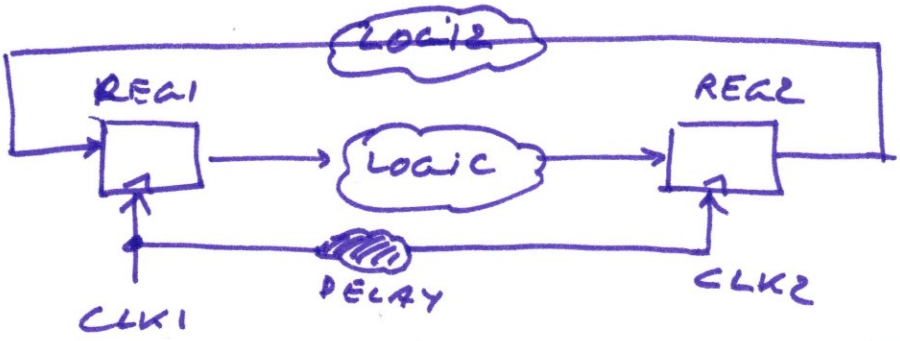
(2) $t_{HOLD} + t_{SKEW} < t_{CQ} + t_{Logic}$

$t_{HOLD} < t_{CQ} + t_{Logic} - t_{SKEW}$ BAD!

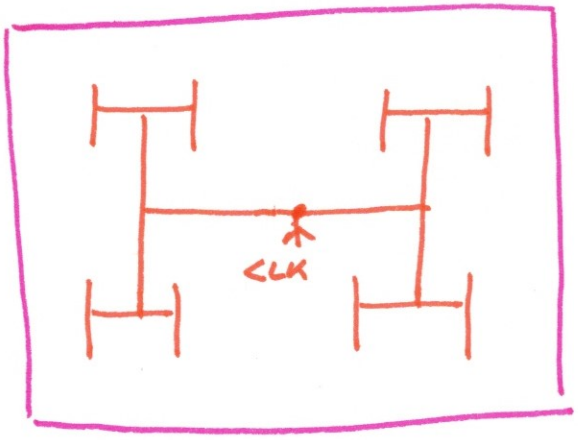
POSITIVE SKEW:



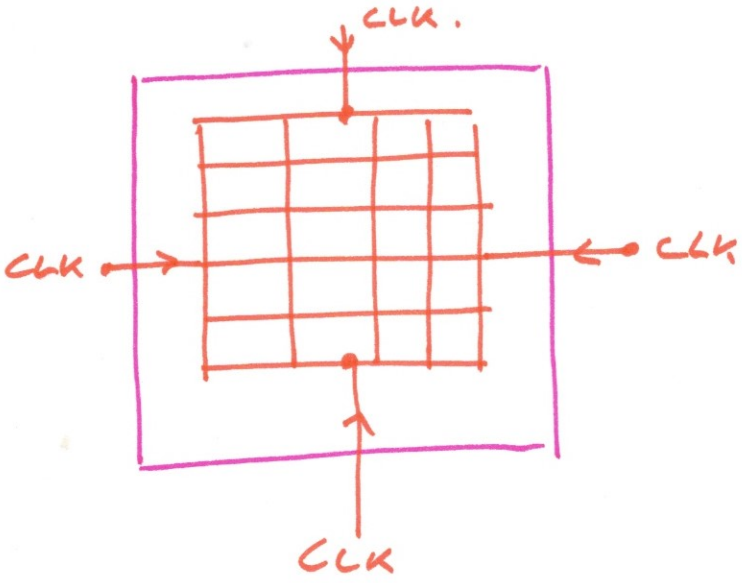
NEGATIVE SKEW:



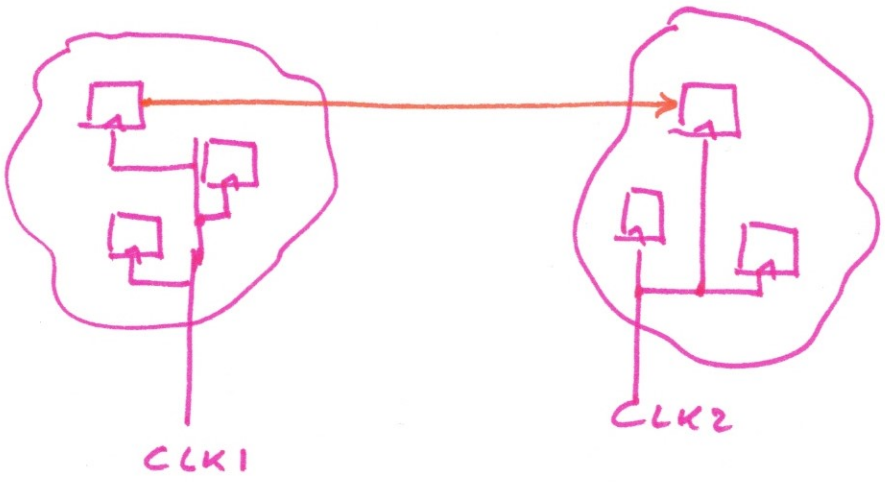
CLOCK DISTRIBUTION

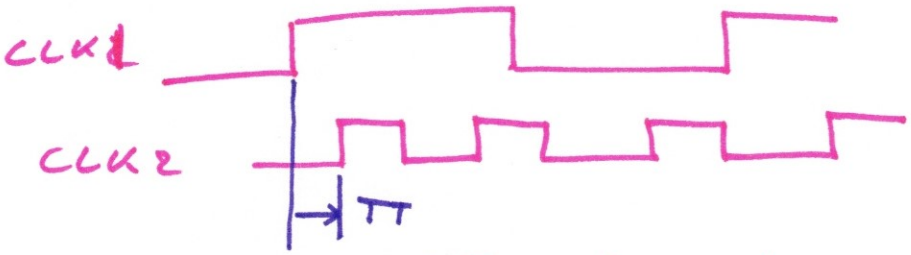


H-TREE



CLK DOMAINS



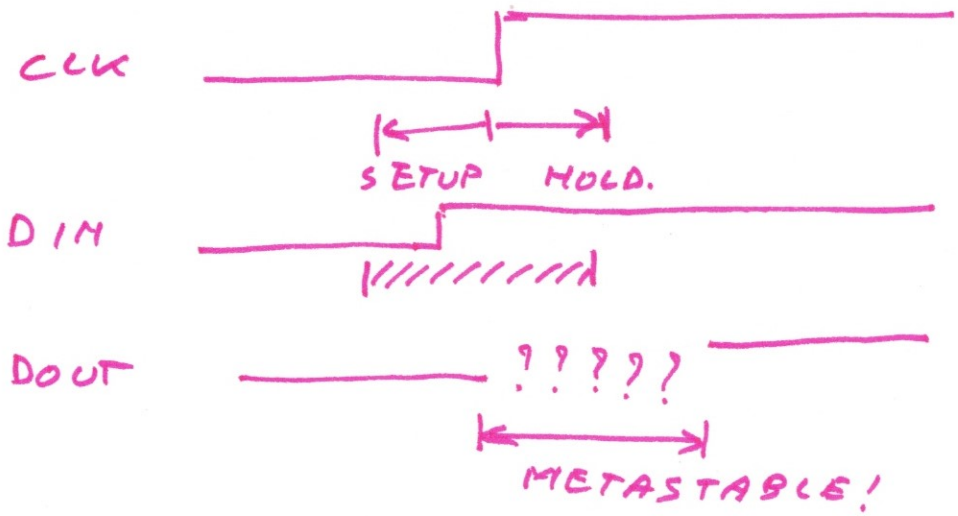


$TT > t_{ca} + t_{LOGIC} + t_{SETUP}$

WHAT HAPPENS @ TIMING VIOLATION?

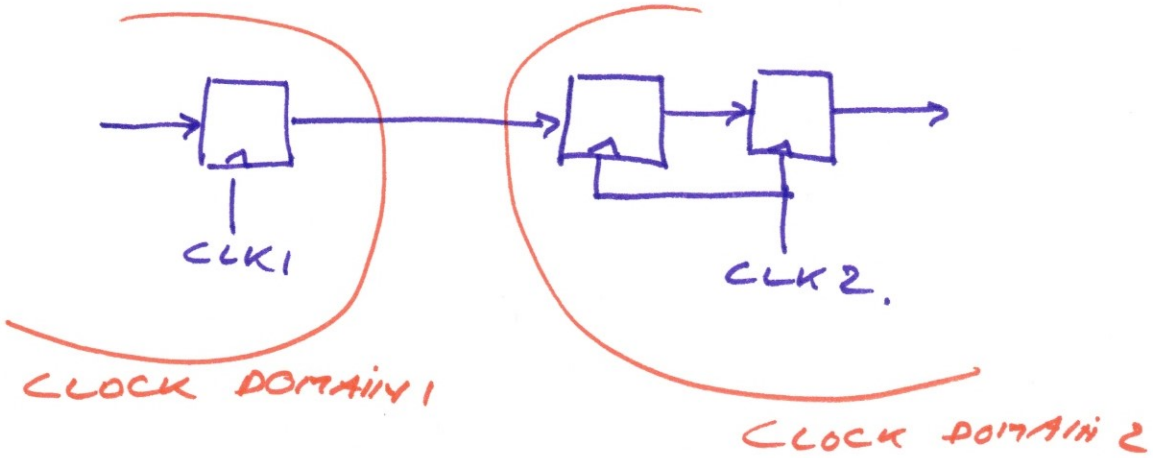
METASTABILITY

- NEITHER 0 NOR 1
- EVENTUALLY CONVERGES TO 0 OR 1

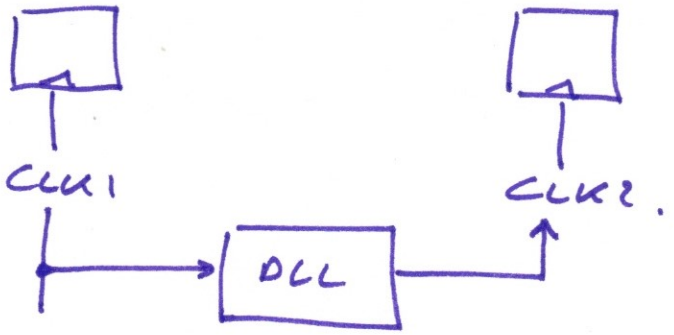


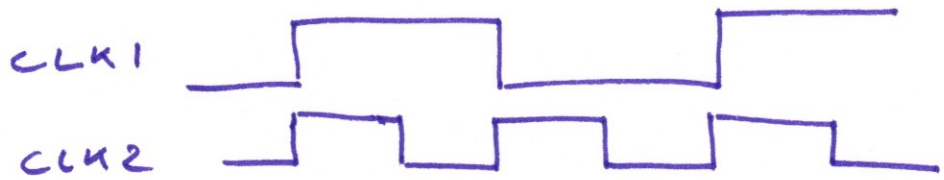
CLK DOMAIN CROSSING

SOLUTION #1 USE SYNCHRONIZER

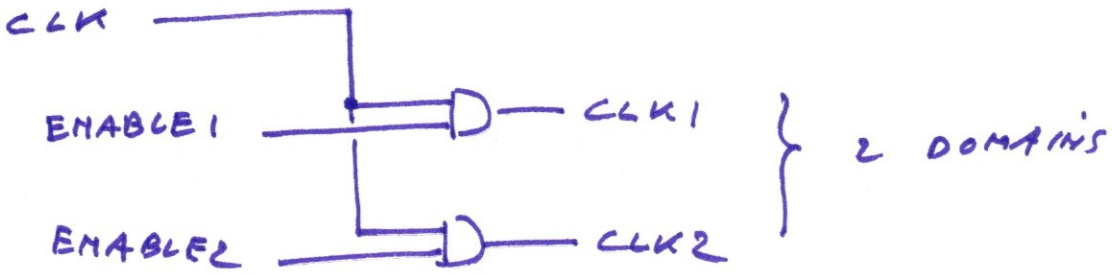


SOLUTION # 2 USE PHASE CONTROL.
(USE DLL)





CLOCK GATING



IN FPGA: