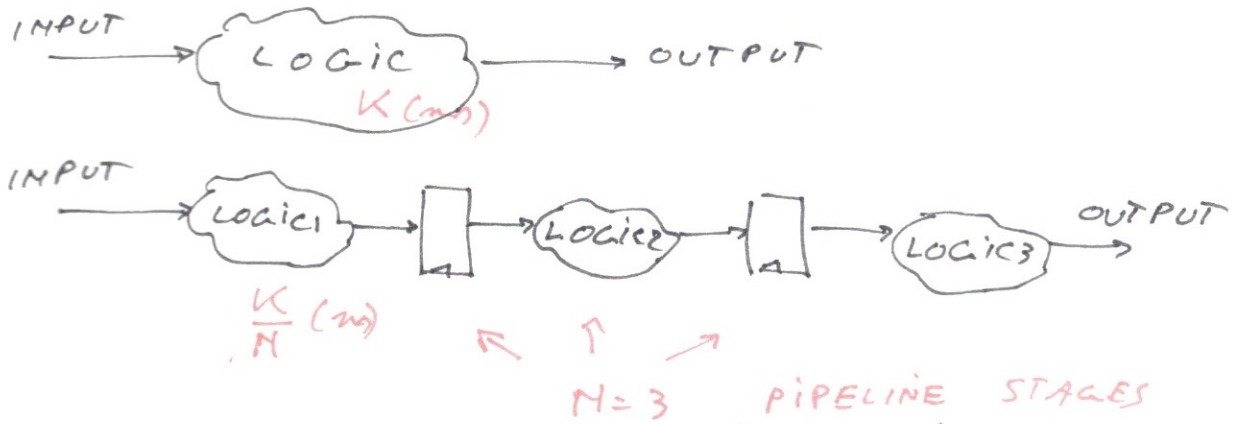


PIPELINING

(1)



	ORIG	PIPELINED
1) LATENCY	1	3 (CYCLES)
2) CRITICAL PATH	K	$K/3$
3) THROUGHPUT	$\frac{K}{N}(s)$	3. $\frac{K}{N}(s)$

RESERVATION TABLE

	0	1	2	3	
Logic1	X	Y	Z		
Logic2		X	Y	Z	
Logic3			X	Y	Z

EXAMPLE OF A NON LINEAR PIPELINE

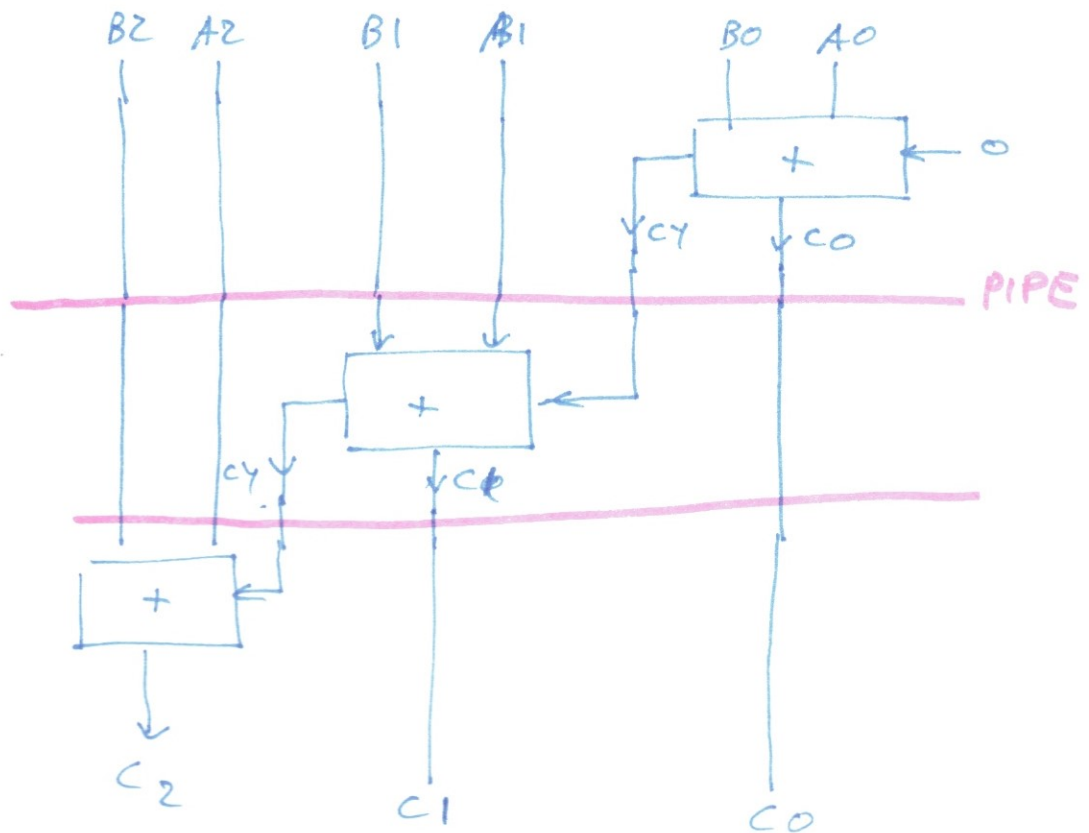
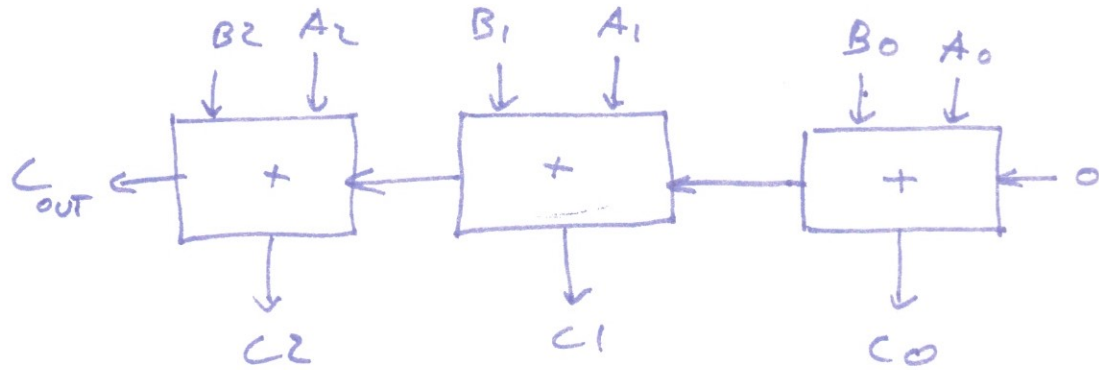
→ 1 OR MORE STAGES ARE REUSED

	0	1	2	3	4	5	6	7
LOGIC1	X	Y			Z			
LOGIC2		X	Y	X	Y	Z		Z
LOGIC3			X	Y			Z	

PIPELINED CIRCUITS

2

RIPPLE CARRY ADDER



MULTIPLIER

3

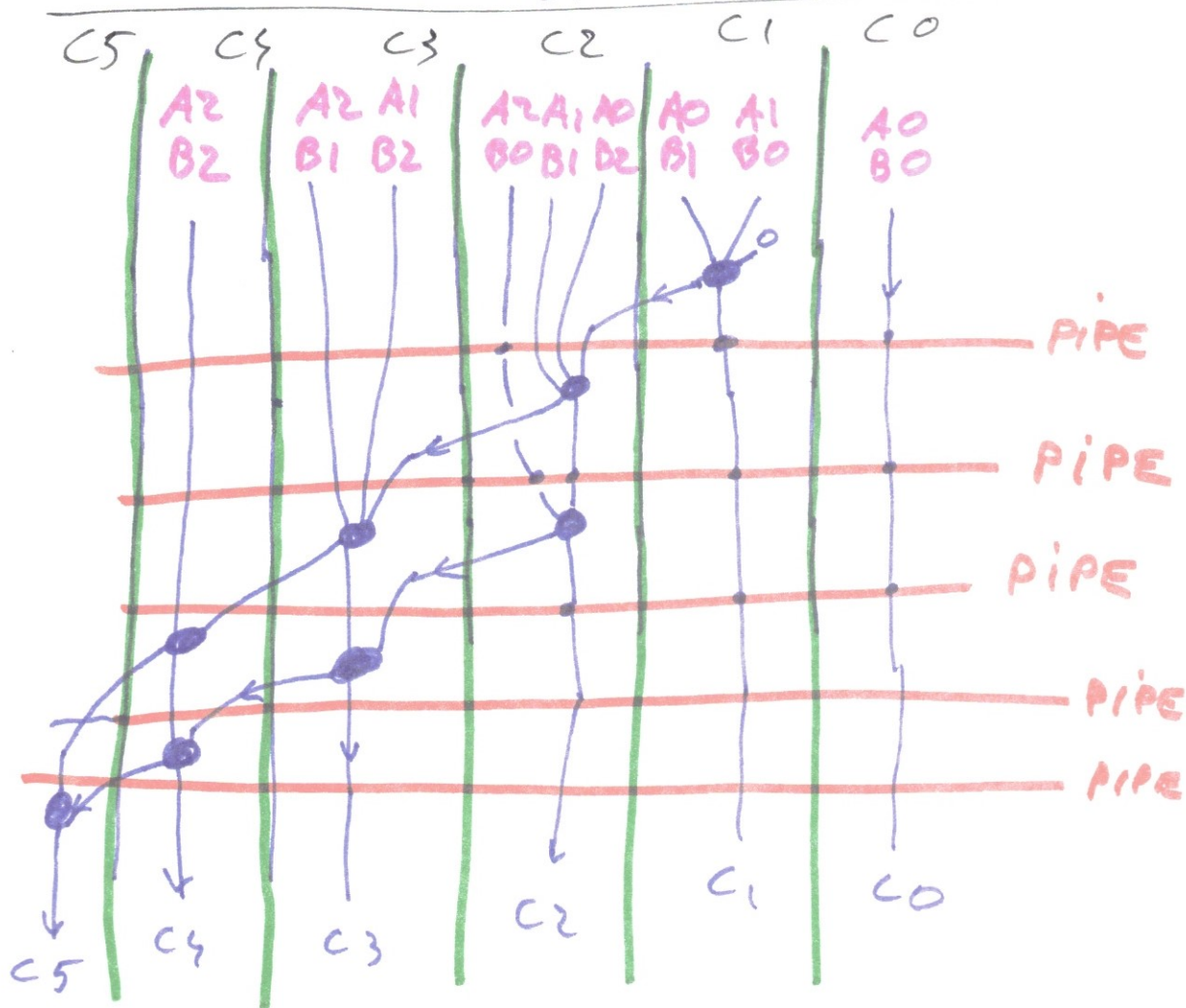
A2	A1	A0
B2	B1	B0

A2B0	A1B0	A0B0
------	------	------

A2B1	A1B1	A0B1
------	------	------

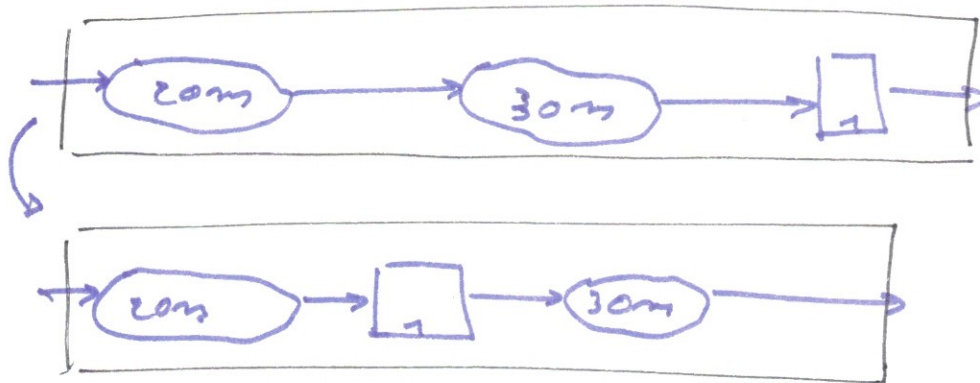
A2B2	A1B2	A0B2
------	------	------

CY	A2B2 + CY	A2B1 + A1B2 + CY	A2B0 + A1B1 + A0B2 + CY	A1B0 + A0B1	A0B0
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RETIMING

9

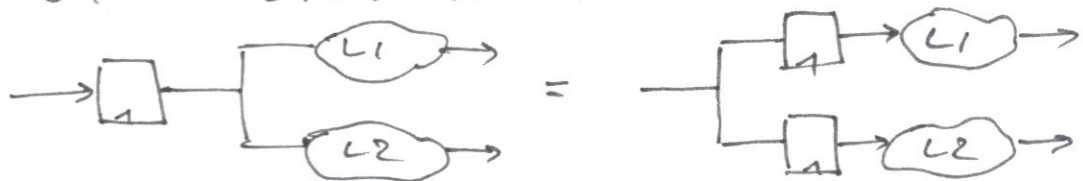


3 RULES

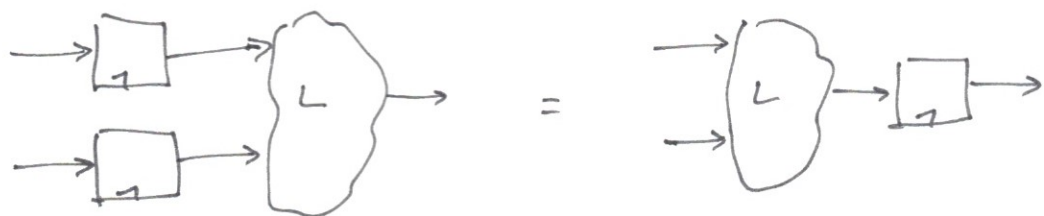
1) REGISTERS CAN MOVE ACROSS LOOP-FREE LOGIC



2) REGISTER CAN MOVE INTO A FORK BY DUPLICATING IT



3) REGISTER CAN MERGE INTO A FORK BY DE-DUPLICATING IT



EXAMPLE 1

5



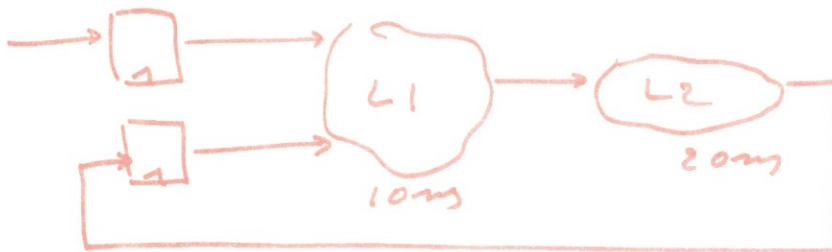
$$t_{CRIT} = 30m$$



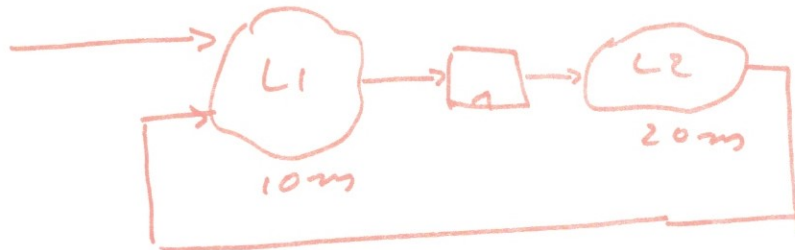
$$t_{CRIT, RETIMED} = 20m$$

RETIMED

EXAMPLE 2



$$t_{CRIT} = 30m.$$



$$t_{CRIT, RETIMED} = 30m$$

RETIMED

