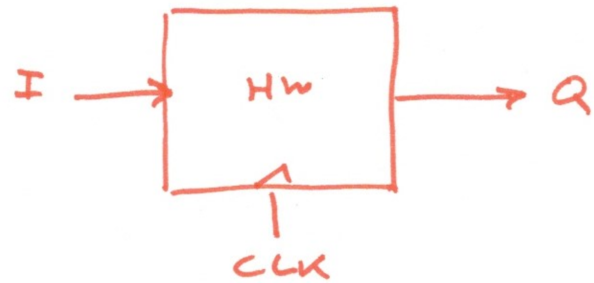
TIMING ANALYSIS

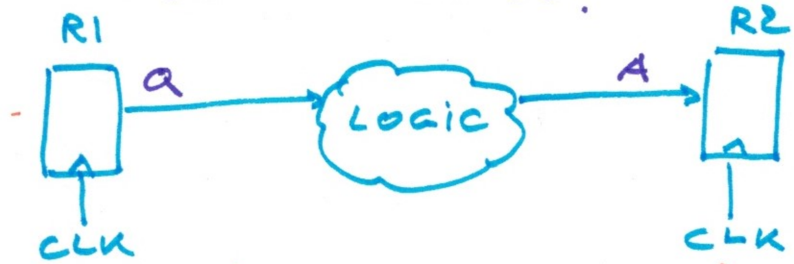


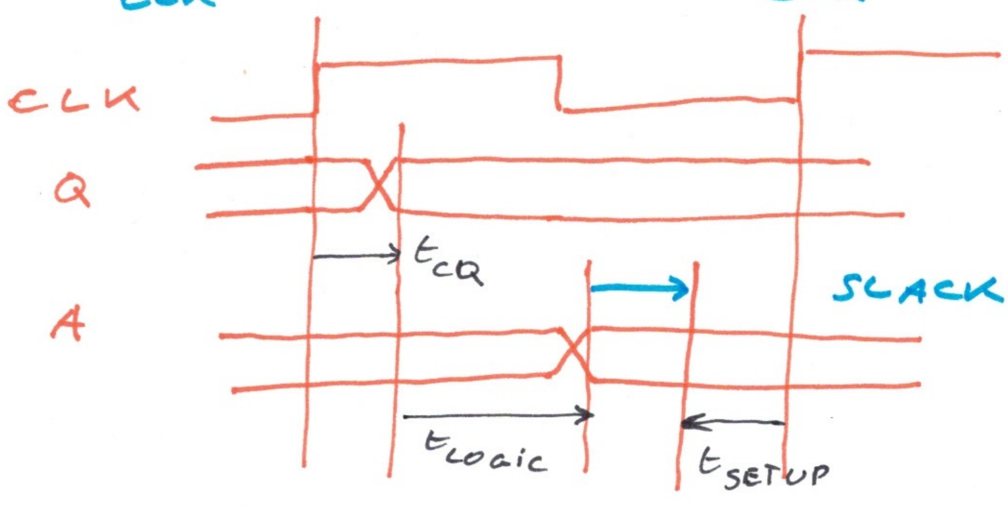
(S) LATENCY: TIME TO COMPUTE Q FROM I

(S^{-1}) THROUGHPUT: THE RATE AT WHICH Q'S ARE PRODUCED

DELAY = $\underbrace{\text{\# CYCLES}}_{\text{DETERMINED BY VERILOG CODE}} \times \underbrace{\text{CLOCK PERIOD}}_{\text{TECHNOLOGY DEPENDENT}}$

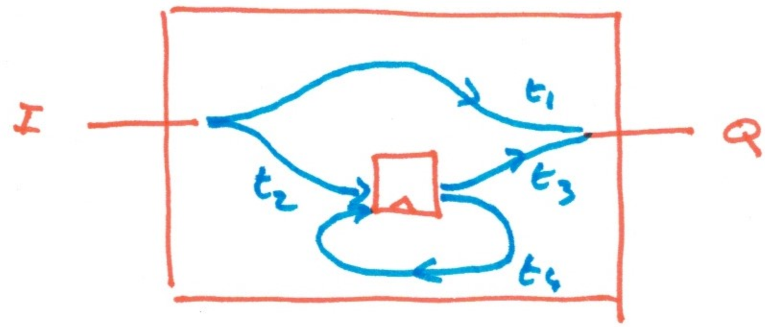
MINIMUM CLOCK PERIOD?





$$T_{CLK,MIN} = t_{CQ} + t_{LOGIC} + t_{SETUP}$$

TIMING ANALYSIS



CRITICAL PATH = MAX (t_1, t_2, t_3, t_4)

lecture10 - Timing Analysis

EXAMPLE I

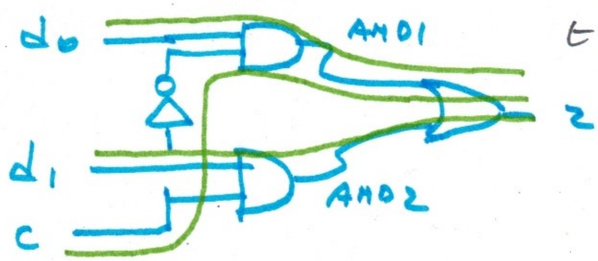
```
    module mux(input wire d0,
               input wire c0,
               input wire d1,
               output wire z);

    wire and1, and2, not1;

    assign z = and1 | and2;
    assign and1 = d0 & not1;
    assign and2 = d1 & c;
    assing not1 = ~c;

    endmodule
```

t_{NOT}
t_{AND}
t_{OR}



$t_c = t_{NOT} + t_{AND} + t_{OR}$

$t_{d_1} = t_{AND} + t_{OR}$

$t_{d_0} = t_{AND} + t_{OR}$

$t_{CRIT} = MAX(t_c, t_{d_1}, t_{d_0})$

EXAMPLE II

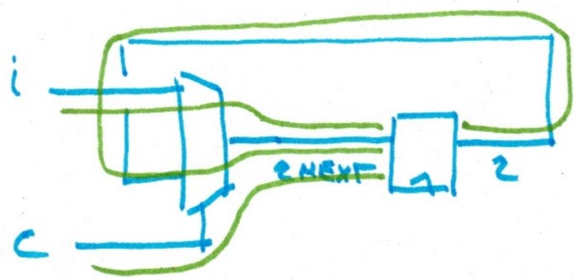
```
  module accum(input wire i,
               input wire c,
               input wire clk,
               output wire q);

   reg r, rnext;

   always @(posedge clk)
     r <= rnext;

   always @(*)
     rnext = c ? i : r;

  endmodule
```



t_{MUX}
t_{CQ}
t_{SETUP}

$t_C = t_{MUX} + t_{SETUP}$

$t_I = t_{MUX} + t_{SETUP}$

$t_R = t_{SETUP} + t_{CQ} + t_{MUX}$

$t_{CRIT} = MAX(t_c, t_I, t_R)$

EXAMPLE III

```
module fir(input wire clk,
           input wire [3:0] i,
           output wire [3:0] y);

  reg [3:0] tap1, tap1next;
  reg [3:0] tap2, tap2next;
  reg [3:0] c1, c2, c3;
  reg [3:0] a1, a2;

  always @(posedge clk)
    begin
    tap1 <= tap1next;
    tap2 <= tap2next;
    end

  always @(*)
    begin
    c1       = i    * 5;
    c2       = tap1 * 3;
    c3       = tap2 * 2;
    a1       = c1 + c2;
    a2       = a1 + c3;
    tap1next = i;
    tap2next = tap1;
    end

  assign y = a2;

  endmodule
```