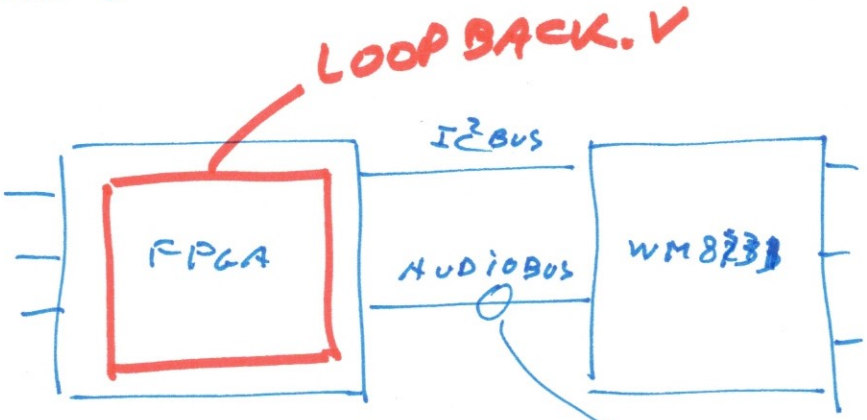
THE STORY SO FAR:

- FSM
  - ALWAYS @(POSEDGE CLK)
    ALWAYS @(*)
  - REGISTERS MODELED AS 2 REG
  - DEFAULT ASSIGNMENT ON ALL VAR IN ALWAYS(*)
  - DEFAULT CASE
  - INSTANTIATE MODULES W NAMED PORT ASSIGNMENT

- EXTENSIONS FSM
  - HIERARCHICAL FSM
  - FSM W DATAPATH
  - DATA CLOCKS

HOMEWORK 2

HOMEWORK 3



① I^2C PROGRAMMING
② CLOCK GENERATION
③ AUDIO FORMAT
④ WAVEFORM GENERATION