01/22/19 03:17:53 C:\cygwin\home\ece4514s19\heartbeatde1soc\heartbeatde1soctb.v

```
1  `timescale 1ns/ 1ns
2
3  module heartbeatde1soctb;
4
5    reg CLOCK_50;
6    reg CLOCK2_50;
7    reg CLOCK3_50;
8    reg CLOCK4_50;
9
10   wire [9:0] LEDR;
11   reg [3:0] KEY;
12
13   heartbeatde1soc dut(CLOCK2_50,
14                       CLOCK3_50,
15                       CLOCK4_50,
16                       CLOCK_50,
17                       KEY,
18                       LEDR);
19
20   always #10 CLOCK_50 <= ~CLOCK_50;
21
22   initial
23     begin
24       $monitor("t=%8d LEDR=%10b", $time, LEDR);
25       CLOCK_50  <= 0;
26       CLOCK2_50 <= 0;
27       CLOCK3_50 <= 0;
28       CLOCK4_50 <= 0;
29       KEY <= 4'hf;
30       #500 KEY[0] <= 0;
31       #1000 KEY[0] <= 1;
32     end
33
34 endmodule
```

CLOCK50 ... KEY[0]

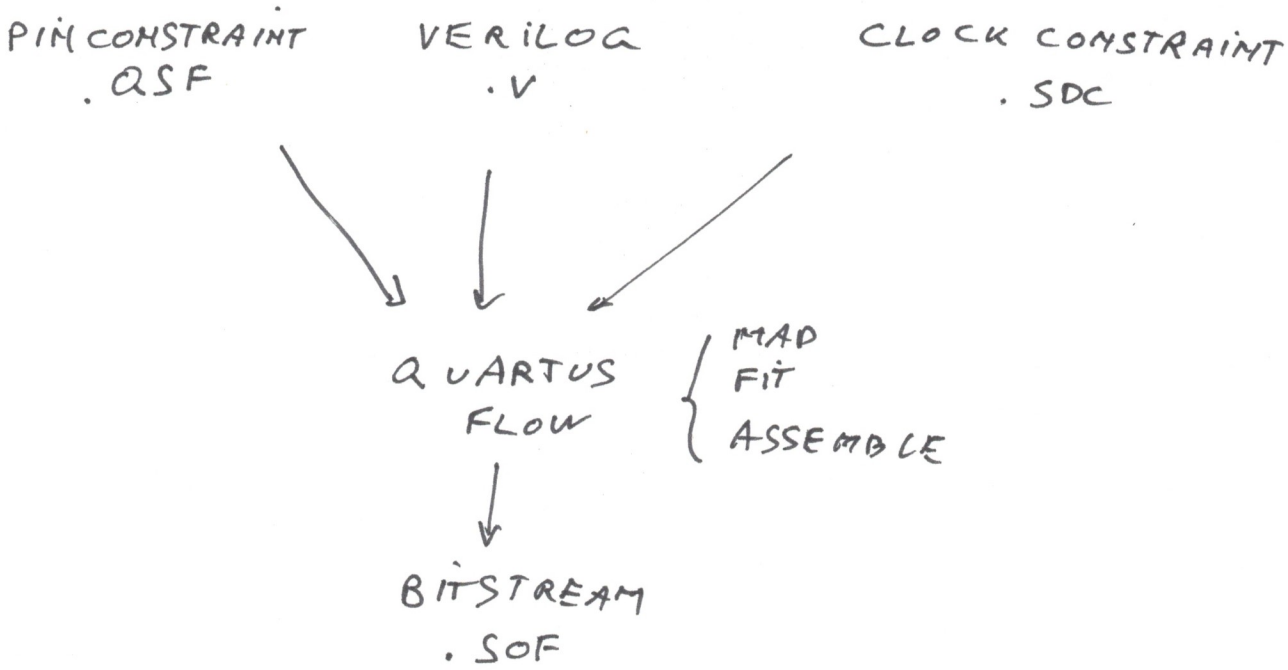
DUT

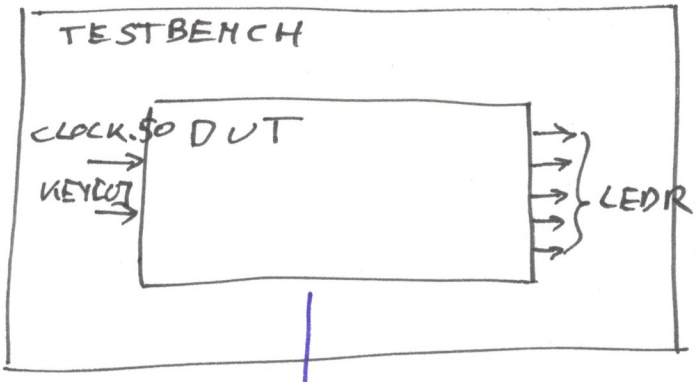
LEDR

STIMULI

#20000 $FINISH;

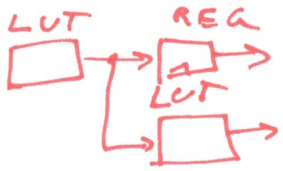
TIME	0	10	20	....	500	510	....	1500	1510
CLOCK_50	0	1	0		0	1		0	1
KEY	1	1	1		0	0		1	1
COUNT_REG	X	X	X		X	0		0	1

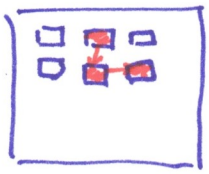

PIN CONSTRAINT
.QSF
VERILOG
.V
CLOCK CONSTRAINT
.SDC
QUARTUS
FLOW
MAP
FIT
ASSEMBLE
BITSTREAM
.SOF



→ SIMULATION OK!

SYNTHESIS





MAP

FIT
- PLACEMENT
- ROUTING

ASSEMBLE

BITSTREAM