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Outline

Thermal Covert Channel Filtering

- On-chip heat generation and detection
- Optimized detection using DSP
- Thermally indifferent PUF
 - Temperature Effects on PUF
 - Mitigating Temperature Effects
 - Area Optimized solution
- Measuring lots of (FPGA) chips ...

Covert Channel based on Heat



Bandwidth ~ 0.0138 bps

Brouchier, Kean, Marsh, Naccache, "Thermocommunication," ePrint IACR 2009/002

How *covert* can we make it?

- Temperature profile on an FPGA over 1 day
 - On-chip temperature measurement
 - We touched the FPGA package two times for a few seconds. Can you see when?



How touching a package affects T



Pedram, Nazarian, "Thermal Modeling, Analysis, and Management in VLSI Circuits: Principles and Methods," Proc. IEEE, August 2006

Can information be more covert?

- Detecting Temperature *events* on an FPGA
 - SNR of 24-hour measurement is very poor
 - The energy in the event of interest if very small
 - But the event of interest may be band-limited !



Our communications system



- We need
 - A good sensor: sensitive, high bandwidth
 - A good detector

Bandwidth and Resolution of Sensors

| CLASSIFICATION OF TEMPERATURE MONITORING | D 1 111 | Lateral | Temperature |
|--|------------|------------|-------------|
| METHODS | Bandwidth | resolution | resolution |
| NON EMPEDDED METHOD | | resolution | resolution |
| NON EMBEDDED METHOD | | | |
| NON CONTACT METHODS | | | |
| Infrared emission thermography | 50 kHz[23] | 10 µm[1] | 0.02°C[24] |
| Thermoreflectance | 150 MHz | 0.5 μm | 0.001°C |
| Interferometry | 150 MHz | 0.5 µm | 1 fm ~ |
| | | · | 0.0001°C |
| CONTACT METHODS | | | |
| Liquid crystal thermography[25,67,68] | 0.01 Hz | 1 μm | 0.1°C |
| Fluorescent microthermography[4] | 0.01 Hz | 0.7 μm | 0.01°C |
| Scanning Thermal Microscopy[26] | 100 kHz | 50 nm | 0.001°C |
| EMBEDDED METHODS | | | |
| Absolute temperature sensors | >1 MHz | No | |
| Differential temperature sensors[6] | >1 MHz | No | 0.01 °C |
| | | | |

Altet, Claeys, Dilhaire, Rubio, "Dynamic Surface Temperature Measurements in ICs," Proc. IEEE, August 2006.

Ring-oscillator based Thermal Sensor

Sample a Free-running Ring Oscillator



Ring-oscillator based Thermal Sensor

How good is this structure in detecting temperature variations?



- Detection bandwidth is limited by f_s/2
- However, a high f_s is not ideal either –Processing load
- Digital RO cannot be alias-free

Our communications system



Select band based on expected signal



Select band based on expected signal



After Filtering





- 1. Suitable filtering based on DSP drastically increases sensitivity
- 2. Chip Temperature Sensors can have a high bandwidth (~MHz)

(Open issue: how well can this be exploited with simple on-chip sensors?)

or:

(Can thermal sensors be used for sidechannel analysis as well?)

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RO-based PUF



Self-Heating

Ensure RO's use low duty factor



S. Lopez-Buedo et al, "Thermal Testing on Reconfigurable Computers," IEEE Design and Test, 4-11, Jan-Mar 2000.

Temperature Dependence



S. Lopez-Buedo et al, "Thermal Testing on Reconfigurable Computers," IEEE Design and Test, Jan-Mar 2000.

Temperature Dependence



S. Lopez-Buedo et al, "Thermal Testing on Reconfigurable Computers," IEEE Design and Test, Jan-Mar 2000.

Brute-forcing stability

- Instead of comparing a pair of RO, consider a group of RO
 - Use only the maximum or minimum f [Suh 2007]
- This reduces the useful C/R space
- In turn, this leads to larger PUFs (more RO's), higher cost

Compact, stable RO

Configurable Ring Oscillator



8 RO for the price of one

- Configurable Ring Oscillator
 - Fits in a single CLB, uses only local routing
 - Reproducible macrocell



Selecting the Configuration



Tuning:

a/ Apply each configuration {c0, ..., c7} to A *and* B (this removes all dependencies on routing)

b/ Determine and store the configuration g(A,B)=j for which maximum absolute frequency difference is obtained

Usage:

Each time pair A, B is compared, select configuration j

C/R Strategy for 128 RO

- Fixed C:
 - Pairwise comparison of adjacent RO pairs
 - Compensate for correlated effects



CLB Columns

Measurements on 128-RO PUF

Unstable bits



Remember

- 1. Architecture Optimization can simultaneously address PUF stability and resource cost
- 2. Increasing PUF stability will simplify postprocessing (*helper data processing*)

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Recent PUF work

Hard to get PUF performance data for large populations (> 100 chips)

| Table 1: Previous work on experimental FPGA Variability Analysis | | | | | | |
|--|-------------|-------------|----------|---------------|------------|--|
| Researcher | Die-to-die | Within-die | Circuit | Technology | Population | |
| | Measurement | Measurement | | (nm) | | |
| Sedcole [15] | yes | yes | Ring Osc | 90 | 18 | |
| Kassapaki [19] | yes | no | Delay | 150 | 4 | |
| Onodera [20] | yes | yes | Ring Osc | 90 | | |
| Suh [21] | yes | yes | Ring Osc | 90 | 15 | |
| Guajardo [22][23] | yes | yes | SRAM | 90 | 2 | |
| Kumar [25] | yes | yes | Latch | 65 | 36 | |
| Maes [26] | yes | yes | Delay | 130 & 90 | 9 & 20 | |
| Holcomb [27] | yes | yes | SRAM* | 90 | 8 | |
| * standalone SRAM chips attached to an FPGA rather than on-chip SRAM | | | | | | |

NSF Project

• Infrastructure to collect and analyze circuit variability in FPGAs

