# Digital Upconversion Architecture for Quadrature Modulators

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**Abstract - Traditionally, the digital implementation of modems is restricted to parts operating at baseband frequency. At higher frequencies, roughly 30 MHz and beyond, analog technologies such as SAW filters provide a better power/performance figure [1]. In this paper, we show how this barrier can be broken by trading programmability for speed. Using a digital multirate filter structure that offers combined interpolation and frequency shifting, an area- and power efficient digital upconversion is achieved.**

## INTRODUCTION

In recent years, digital modems for broadband networks have gained major interest [2]. Examples of such target networks currently embedded are telephone twisted pair [3] and fiber-coax CATV [4]. The modems inside these networks need to operate in a strongly regulated environment and cannot interfere in present network operation. Among other, this puts down two requirements

- Flexible setting of the modulation carrier frequency is needed. This allows to adapt one modem for different network types.
- High spectral efficiency is required, in order to achieve maximal data throughput for a minimal network bandwidth occupation.

Typical characteristics of such access modems are shown in table 1. The first requirement for these modems is achieved using double conversion, which splits modulator operation and carrier frequency setting. The second requirement is met by choosing an efficient modulation scheme. In the next section, the traditional channel positioning approach using the double conversion architecture is discussed. This will reveal that the digital implementation is restricted to baseband frequencies. Next, we present alternative approaches that allow the upconversion part of the channel positioning to be done digitally. This offers a higher integration without recurring to mixed-signal technology, which is more difficult to test than an all-digital implementation. Following this, a digital upconversion architecture is elaborated. Simulation

| Application | Media | Bandwidth (MHz) | Bit Rate (Mbit/s) | Carrier (MHz) | Spectral Efficiency (b/s/Hz) | Modulation |
|---|---|---|---|---|---|---|
| ADSL Downstream | Twisted Pair | 1 | 6 | 0.55 | 6 | DMT |
| ADSL Upstream | Twisted Pair | 0.1 | 0.6 | 0.55 | 6 | DMT |
| Set-top Upstream | HFC | 3 | 10 | 5 - 30 | 3 | QAM |

Table 1: Typical parameters of access network modems

and synthesis results are given along with power estimates, followed by the final conclusions.

For illustration purposes, a 12 $Mbit/s$ QAM-16 (quadrature amplitude modulation) modem architecture is assumed. The results however are modulation-type independent and can be easily extrapolated to other modem architectures.

# DOUBLE CONVERSION ARCHITECTURE

A double conversion architecture allows a QAM modulator to operate at fixed carrier frequency. It takes the following steps.

**1.** Generation of a complex baseband or low-IF (intermediate frequency) QAM signal.

**2.** Upconversion of this modulated band to IF.

**3.** Downconversion of the modulated band to the desired channel frequency.

The IF must by chosen such that it lies well outside the projected transmission band (table 1). This prevents mixer image band interference during the double conversion.

Digital implementation of the modem baseband functions inevitably leads to the problem of alias band removal after D/A conversion. This can be done by lowpass filtering of the baseband QAM modulation. Alternatively, alias band removal can be done at IF. The anti alias filter then can be combined

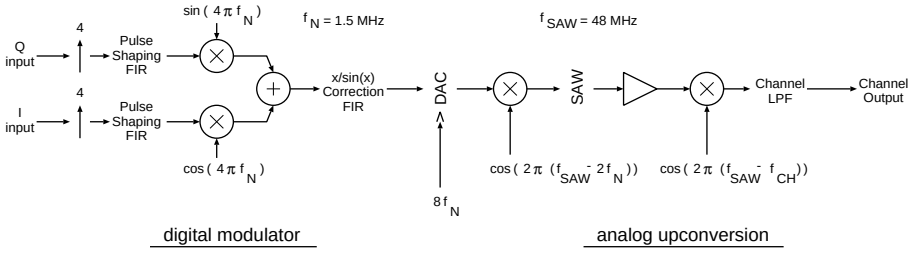



Figure 1: Conventional Double Conversion Architecture

with the upconversion image reject filter. This requires a high-Q filter, because of the steep QAM modulation band edges. A SAW filter can offer such a Q-factor.

The typical analog upconversion system architecture is shown in the figure 1. The system starts in the digital domain at complex baseband. The digital QAM modulator contains digital pulse shaping FIR filters for both the I and Q branches. The root raised cosine pulse shape responses are sampled at 8 times the Nyquist rate $f_N$ (4 samples per symbol).

The complex baseband signal is upconverted digitally to a carrier frequency of 2 times the Nyquist frequency. As this frequency conversion involves sine and cosine values of $\frac{\pi}{2}$ multiples only, it is easily implemented.

Next, the modulation is passed to a $x/sin(x)$ correction filter [6] and converted to an analog signal using a D/A converter sampling at 4 times the symbol rate. Next, the signal is upconverted to IF, which is located at the center frequency of a SAW filter, in this case 48 MHz. This upconversion is performed using an analog mixer. After alias band removal, an amplifier compensates the insertion loss of the passive SAW filter. Then, a downconversion to the desired channel carrier frequency is done using a second analog mixer. Finally, a lowpass filter removes the downconversion image band located at high frequencies.

In order to lower part count, higher integration is needed. This can be done by shifting the digital boundary towards the modulator output. This is the topic of the next section.

# DIGITAL UPCONVERSION

In a digital upconversion system, we aim at generating the digital carrier at the center frequency of the SAW (48 MHz). For this purpose, a sample rate of roughly 120 MHz is needed. Further digital integration past the SAW filter is not useful. It introduces an additional anti alias filter and increases the system part count again.

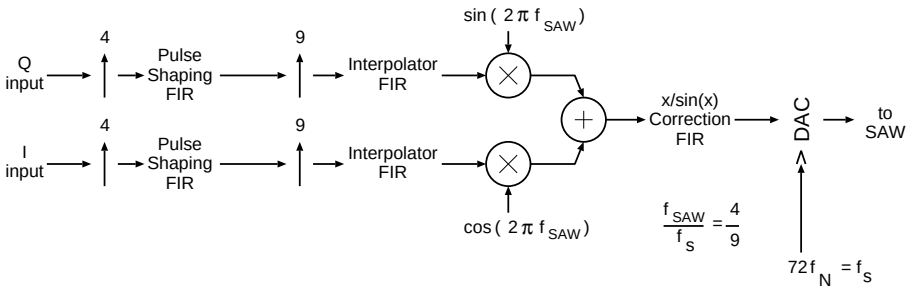



Figure 2: Digital Modulator and Upconversion Architecture

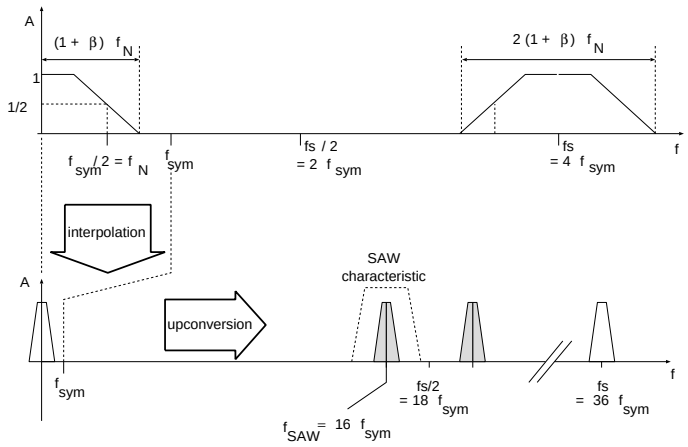



Figure 3: Digital Upconversion Output Spectrum

This high sample rate is however not needed throughout the digital system. By using an interpolator structure after the QAM pulse shaping filters, followed by a digital mixer, the high sample rate is restricted to the last parts before D/A conversion. This yields an architecture as shown in figure 2.

If the SAW center frequency is selected to be an integral multiple of the symbol frequency, an efficient architecture can be obtained. In figure 3, the SAW center frequency is shown to be located at 16 times the symbol frequency $f_{sym}$. The modulation bandwidth varies, with the rolloff factor, between 1 and 2 times the symbol frequency $f_{sym}$. Thus, the interpolator filter should bring $f_s/2$ to at least 18 $f_{sym}$ in order to offer alias-free representation of the modulation band at the SAW center frequency. Because the sample rate at the interpolator input is $4.f_{sym}$, an interpolation factor of $2.18f_{sym}/4f_{sym} = 9$ meets the requirements.

After increasing the sample rate, an upconversion using a quadrature mixer is done. This brings the carrier frequency from DC to the SAW center frequency, at 16 times the symbol rate. The upconversion is done by multiplying the interpolator filter output with a complex phasor rotating at carrier frequency. Because the carrier frequency is a rational factor of the sample rate $f_s$ (4/9), digital generation can be done efficiently.

The digital upconversion problem has two aspects:

- Design of an interpolator structure that offers a ninefold sample rate increase.
- Design of a digital mixing process with a carrier frequency of 4/9 $f_s$.

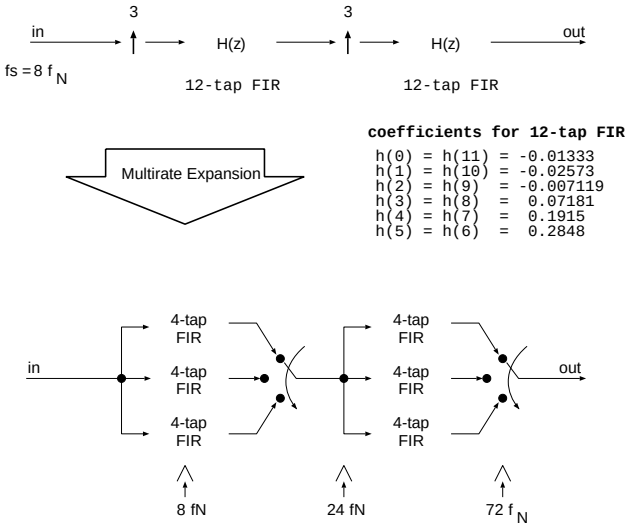



Figure 4: Interpolator Filter Structure

## Interpolator Design

For interpolation of QAM modulation, linear phase filters are needed to avoid the introduction of group delay distortion. Such interpolator filters have been well documented in literature as multirate structures [7],[8]. The complexity of these is determined by the interpolation factor, and the bandwidth utilization of the interpolated signal. Various configurations have been tested, and a two step interpolation filter has been retained, as shown in figure 4. The filter coefficients were obtained using a Parks-McClellan algorithm [9].

## Conventional All-Digital Upconversion

A digital oscillator/ mixer architecture can be implemented in various ways. One common all-digital solution to our problem will be described.

First, the carrier phase is generated using a modulo-9 counter with a step of 4. Out of this carrier phase, sine and cosine values are derived to construct a complex phasor by which the complex baseband signal can be multiplied.

The sine and cosine values are stored in a 9 entry lookup table, and implemented as a PLA or ROM. The resulting values are fed into a complex digital full-multiplier, operating at the high sample rate (36 * 3 MHz = 108 MHz). Bit-level pipelining of the multipliers is mandatory at this high speed. By having the step of the modulo-9 counter variable, a certain carrier flexibility is obtained. This flexibility comes at the cost of complex hardware running at high speed. However, as the SAW center frequency is fixed, the carrier tuning is not utilized, and we obtain a power-ineffective solution.

An approach that makes uses of this manifest property is considered next.

## Proposed All-Digital Upconversion

As the SAW frequency is fixed, the upconversion operation can be coded into the interpolator filter coefficients.

The correct coefficients and filter structure are derived using the Z-transform. The system structure, shown in figure 5, behaves as follows. Given the output sample stream of the matched filters, we form a complex sample stream

$$x_k = i_k + jq_k \tag{1}$$

which has a Z-transform

$$X(z) = \sum_{k=0}^{\infty} (i_k z^{-k} + jq_k z^{-k}) \tag{2}$$

Increasing the sample rate ninefold yields $X_{up}(z)$

$$X_{up}(z) = X(z^9) = \sum_{k=0}^{\infty} (i_k z^{-9k} + jq_k z^{-9k}) \tag{3}$$

This signal is processed by the interpolator filter structure, which has a transform $G(z)$. The signal at the interpolator filter output equals

$$\mathcal{Z}\left(y(t)\right) = Y(z) = G(z)X_{up}(z) = G(z)X(z^9) \tag{4}$$

which yields the upconverted signal as

$$\begin{aligned} Y_{up}(z) &= \mathcal{Z}\left(y(t).e^{j2\pi f_{SAW}t}\right) \\ &= Y(ze^{j2\pi\frac{f_{SAW}}{f_s}}) \\ &= Y(ze^{j2\pi\frac{4}{9}}) \\ &= G(ze^{j2\pi\frac{4}{9}}).X(z^9e^{j2\pi\frac{4.9}{9}}) = G(ze^{j2\pi\frac{4}{9}}).X(z^9) \end{aligned} \tag{5}$$

Thus, the upconversion to a frequency which is an integral multiple of $X(z)$'s sample rate avoids the need of additional rotation operations on the input sequence $X(z)$. The upconversion problem is transformed into a coefficient rotation problem. Finally, the signal of interest $Y_S(z)$ is just the real part of $Y_{up}(z)$.

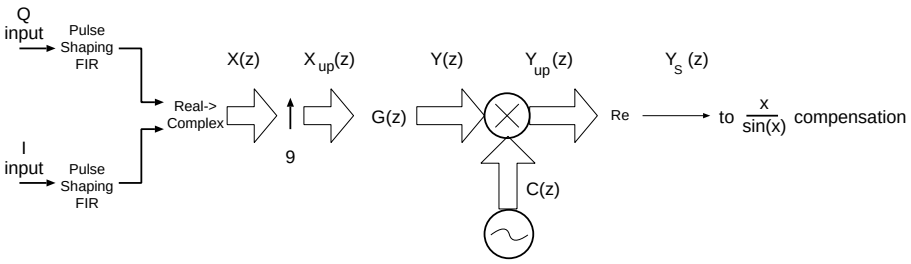



Figure 5: Upconversion Behavior

The impact of the coefficient rotation on the multirate architecture presented previously is examined in the next section.

## Upconversion Implementation

The expansion done in (5) is now applied to the two-stage interpolator filter. The conversion behavior is presented in figure 6.

Relating output and input signals, we find

$$\begin{aligned} Y(z) &= H(z)X_3(z) = H(z)X_2(z^3) \\ &= H(z)H(z^3)X_1(z^3) = H(z)H(z^3)X(z^9) \end{aligned} \tag{6}$$

Comparison (4) and (6) returns the relation between $G(z)$ and the two-stage interpolator

$$G(z) = H(z)H(z^3) \tag{7}$$

Substitution into (5), and using the $2\pi$ periodicity of $f(x) = e^{jx}$ yields

$$\begin{aligned} Y_{up}(z) &= H(ze^{j2\pi\frac{4}{9}})H(z^3e^{j2\pi\frac{4.3}{9}})X(z^9) \\ &= H(ze^{j2\pi\frac{4}{9}})H(z^3e^{j2\pi\frac{3}{9}})X(z^9) \\ &= H_2(z)H_1(z)X(z^9) \end{aligned} \tag{8}$$

The resulting structure is shown in figure 7. One remark is that this structure processes both I and Q branches of the quadrature modulation, whereas the structure of figure 4 processes only one branch. The coefficients of the interpolation filters $H_1(z)$ and $H_2(z)$ can be found out of figure 7.

$$\begin{aligned} H_1(z) &= \sum_{i=0}^{11} h(i)z^{-i}(cos(2\pi\frac{3}{9}i) + j.sin(2\pi\frac{3}{9}i)) \\ H_2(z) &= \sum_{i=0}^{11} h(i)z^{-i}(cos(2\pi\frac{4}{9}i) + j.sin(2\pi\frac{4}{9}i)) \end{aligned} \tag{9}$$

As for implementation cost, it is seen from (9) that the rotated coefficients yield complex values. Thus, the number of constant multiplications to evaluate in each filter is increased from 12 to 48. For the filter at high rate, this

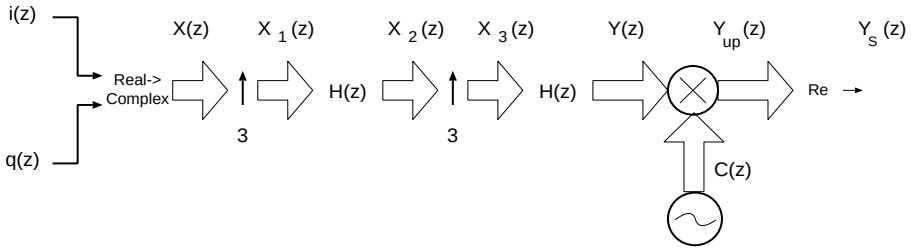



Figure 6: Upconversion Behavior with Multistage Interpolation

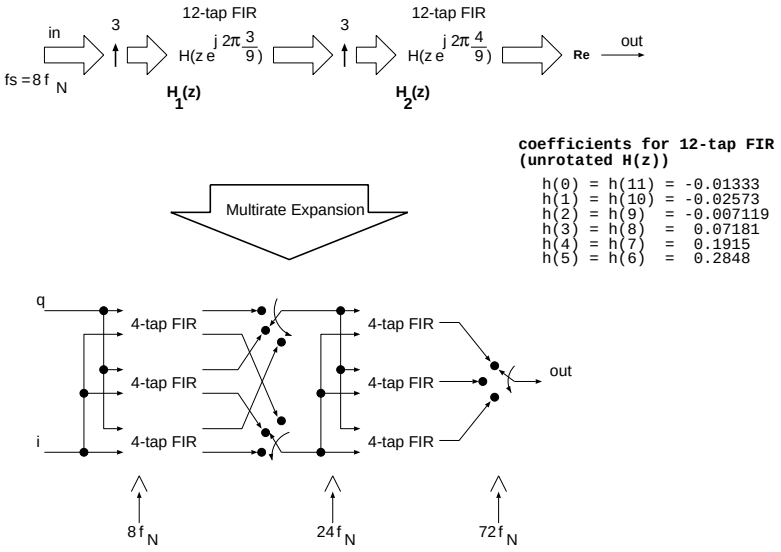
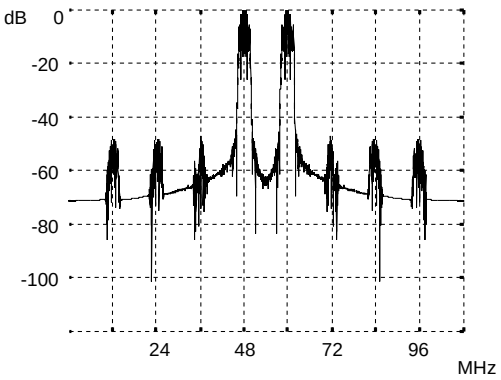



Figure 7: Combined Interpolation/Upconversion Filter Structure

figure is halved because only the real output is needed. We thus need $48 + 24 = 72$ constant multiplications instead of 24. On the other hand, the oscillator/mixer structure is completely integrated in the filter structure, which offers the benefits of multirate implementation. Of the 72 constant multiplications, 48 operate at $8f_N$ and 24 operate at $24f_N$. Only the sincx distortion compensation filter needs to operate at the full rate.

| | Component | Active Area (mm2) | Gate Count | Critical Path (ns) | Power Estimate (mW) | Area x Power (mm2 x mW) |
|---|---|---|---|---|---|---|
| **Proposed Circuit** | $H_1(z)$ | 2.34 | 5318 | 30.4 | 170 | |
| | $H_2(z)$ | 1.26 | 2863 | 27.1 | 140 | |
| | Total | 3.60 | 8181 | | 310 | 1110 |
| **Conventional Approach** | Mix/Osc | 1.14 | 1998 | 7.5 | 330 | |
| | Interpolator | 1.44 | 2512 | 15.8 | 230 | |
| | Total | 2.58 | 4510 | | 560 | 1440 |

Table 2: Area and Power Consumption for the Proposed Filter Structure




| Parameter | Value |
|---|---|
| Master Clock | 108 MHz |
| Technology | CMOS 0.7u 5V |
| Accuracy | 10 bit |
| Power Consumption | 310 mW |
| Active Area | 3.60 mm2 |
| Input Bandwidth (Q or I input) | 2 MHz |
| Output Carrier Frequency | 48 MHz |

Figure 8: Modulator Output Spectrum and Circuit Properties

# RESULTS

The digital upconverter was simulated in C++ and synthesized in hardware using the CATHEDRAL-3 silicon compiler [10]. Figure 8 shows the output spectrum obtained from a floating point simulation of the interpolator structure. The sideband distortions are an effect of the interpolator filter. The 12-tap filter which was selected offers about 45 dB suppression of alias bands. This suppression, added to the SAW stopband suppression, defines the spurious response level of the transmission.

The synthesis was done in a 0.7 micron, 5 Volt CMOS standard cell technology. Internal filter wordlength for $H_1(z)$, $H_2(z)$ was taken 10 bits.

In table 2, area figures, and power estimates are given. The power estimates were obtained by the *Powermill* transistor level timing simulator. Taking the projected clock frequencies into account, a power estimate of 310 mW is found.

A comparison with the conventional all-digital approach was also made. As mentioned before, this approach requires a digital mixer-oscillator operating at 108 MHz, and two interpolator structures as shown in figure 4. Although such a circuit has better area figures than the proposed one, the power consumption as well as the area-power product is worse.

With relation to test, we indicate that the circuits designed with CATHEDRAL-3 are scan-testable. For test observation, the multirate circuit must be clocked single rate. This requires a bypass mode for the clock generation circuit.

Finally, the specifications of the developed circuit are summarized on the right of figure 8.

# CONCLUSION

In this paper, a digital architecture was presented to implement IF upconversion in modems digitally. It offers a lower part count for the resulting system

by means of integration, while keeping at the same time power consumption low.

The technique stresses the benefits of multirate implementation as applied to digital modem design. It also shows the use of manifest design specifications to obtain such an implementation.

## ACKNOWLEDGEMENTS

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