ECE 4530 Hardware/Software Codesign
Fall 2016
Last Update: Mon Aug 22 15:00

Coordinates	
Instructor:	Patrick Schaumont
	schaum@vt.edu
TA:	Daniel Neel
	daniel94@vt.edu
Web:	http://canvas.vt.edu/courses/29254
Email:	ece4530f15@scholar.vt.edu
Meeting Times	
Class	TR 12:30P-1:45P
	NCB 270
Office	TR 2:00P-3:00P
	DUR 337
Office TA	MW 1:00P-2:00P
	CEL/SWEL
	or by appointment

1 Objectives

This course discusses electronic system design at the boundary of hardware and software, considering applications that are realized partially in hardware and partially in software. This includes a study of modeling techniques of hardware and software components at different levels of abstraction and a study of interfacing techniques between hardware components and software components. The course includes homework and practical experiments. Having completed this course, you will have experience in the following.

- Transform simple software programs into cycle-based hardware descriptions with equivalent behavior and vice versa;
- Partition simple software programs into hardware and software components, and create appropriate hardware-software interfaces to reflect this partitioning;
- Analyze and explain the control-flow and data-flow of a software program and a cycle-based hardware description;
- Identify performance bottlenecks in a given hardware-software architecture and optimize them by transformations on hardware and software components;

- Use simulation software to co-simulate software programs with cycle-based hardware descriptions.

2 Equipment and Design Software

- Students will make use of the DE1-SoC Altera Design Kit by Terasic (http://de1-soc.terasic.com). This is a high-performance FPGA board equipped with a Cyclone V SoC Series device; it contains a dual core ARM A9 as well as an FPGA configurable fabric. Students will receive a loaner board, free-of-charge, for the duration of the course. The board must be returned to the department at the end of the semester. Students who fail to return their kit will receive an incomplete (I) grade. Instructions on how to obtain the DE1-SoC board will appear on the course website.
- Students will make use of Altera Quartus Prime Lite v16.0 Design Software, as well as the Altera SoC Embedded Design Software v16.0. This software needs to be installed on a laptop or workstation owned by the student. Quartus Prime includes FPGA design tools and Modelsim HDL simulation. The SoC EDS includes a toolchain for the ARM A9 cores on the FPGA. Installation instructions for this software will be published on the course website. If you have an older edition of this software on your computer, it's a good idea to upgrade it. All assignments and design examples will be made assuming that you have access to Altera Quartus Prime Lite v16.0 and Altera SoC EDS v16.0.

3 Prerequisites

- For undergraduate students, a grade of C or better in each of
  - ECE 3534 (or ECE 2534), Microprocessor-based system design
  - ECE 3504 or ECE 3544, Digital Design I

  I assume that the students in this course will have taken 3544, so that they have a working knowledge of the Verilog Hardware Description Language.
  - I do not recommend to take this course if you are completely unfamiliar with hardware design (ie. have never written a program in Verilog or VHDL before).
  - I do not recommend to take this course if you did not obtain at least C in a prerequisite course.

  The course assumes the following abilities.
  - Knowledge of C programming, assembly programming;

- Knowledge of basic hardware design concepts (Number systems, Combinational and Sequential logic, with applications such as counter modules and arithmetic operations in hardware);
- Basic knowledge of Verilog, including the use of a simulator, and the use of a hardware synthesis tool;
- The ability to undertake a substantial design project.

This course puts a great deal of emphasis on actual design and on learning-by-doing. Students have to be proactive and approach design problems in the manner a design engineer would approach them: by looking for a solution, by thinking before asking questions, by trying before giving up, and last but not least, by not giving up at all.

4 Text and References

- This course will rely on the following textbook:

  Practical Introduction to Hardware/Software Codesign
  Patrick Schaumont
  Springer, 2nd Edition, 2013, xxii+480p
  ISBN 978-1-4614-3736-9 (print)
  ISBN 978-1-4614-3737-6 (online)
  DOI 10.1007/978-1-4614-3737-6

  Students at Virginia Tech can access the PDF of the book online on the SpringerLink website (`http://link.springer.com/book/10.1007/978-1-4614-3737-6/page/1`)

  Please do not post or redistribute the PDFs.

- An optional reference, also available on SpringerLink, is the following textbook. This reference is useful during the first few weeks of the course, when we cover the MSP430 Microcontroller.

  "Introduction to Embedded Systems - Using Microcontrollers and the MSP430"
  Manuel Jimenez, Rogelio Palomera, Isidoro Couvertier
  Springer, 2014, xxiii + 648p
  ISBN 978-1-4614-3143-5 (online)
  DOI 10.1007/978-1-4614-3143-5

  Students at Virginia Tech can access the PDF of the book online on the SpringerLink website (`http://link.springer.com/book/10.1007/978-1-4614-3143-5`)

- An optional reference is the following textbook. It is not available online, but the website contains many Verilog examples for design with the NIOS microcontroller.

"Embedded SoPC Design with Nios II Processor and Verilog Examples"
Pong Chu
Wiley, 2012, 782p
ISBN 978-1-118-01103-4 (print)
Website `http://academic.csuohio.edu/chu_p/rtl/sopc_vlog.html`

- Like last year, the course is undergoing a substantial revision, and most importantly will no longer rely on the GEZEL hardware description language as presented in the book on Hardware/Software Codesign. Instead, all hardware modeling will be done in Verilog. In addition, the software target for this course will include the MSP430 (in the first half of the course) and the ARM A9 core (in the second half of the course).
- Additional reading will be posted on the class website.

5 Assignments

- There will be 8 homework assignments over the semester. The homework assignments will reinforce the class topics. They require you to write programs in C, to develop hardware modules in Verilog, to construct systems with an FPGA design environment.
- Students will also make use of a prototyping environment, a DE1-SoC Altera FPGA board.
- Near the end of the course, a 'Codesign Challenge' will be specified. This is a sample problem that combines all of the above experience in a single project. Students have about two weeks to solve it (Week 13 and Week 14). The results will be discussed in Week 15. A summary of assignments and results from the past years is available at `http://www.faculty.ece.vt.edu/schaum//teaching/4530/`.
- The general policy for assignments is as follows.
  - Except for the codesign challenges, all assignments must be solved within one week. The turn-in schedule will be marked on the handout of each assignment.
  - There is no late policy in this course. Homework assignments have to be posted on the course website before the due deadline of each assignment. *No late policy* means that late Homework gets a zero grade. The exception to this rule are described below under Special Needs.
  - Students are responsible to keep the course equipment (including the FPGA board, the laptop/workstation, and the design software) in good working condition. Technical issues are not a valid reason for a late turn-in.

  - All assignments are individual assignments and must be completed independently by the students. The Forum on the course web site can be used to discuss the assignments within the limits of the Honor Code Policy, provided below.

6 Grading

Semester grades will be based on the following weights.

- Homework (8 in total): 40% of the points
- Codesign Challenge: 25% of the points
- Exams (Midterms and Final): 35% of the points

The exam dates are listed on the tentative schedule included in this syllabus. An exam may be exceptionally rescheduled for an individual student provided a valid reason has been approved by the instructor at least one week before the exam date.

Grading errors on assignments or exams can be appealed within one week after the graded assignment was returned to the student. Appeals must be made to the instructor.

7 Honor Code Policy

Adherence to the Virginia Tech Honor Code is expected in all phases of this course. Any work that you submit for a grade must be your own. Violations will be reported to the Office of the Honor System.

- It is a violation of the honor code to discuss explicit project solutions or exercise solutions.
- All assignments are individual projects and must contain your own work. All external source code material used must be properly cited. It is a violation of the honor code to provide others access to ones' own solution source code. It is also a violation to access other students' solution files.
- Midterm and Final are individual.
- See `http://www.honorsystem.vt.edu` for information about Virginia Tech's Undegraduate Honor System and `http://www.gradhonor.grads.vt.edu` for information about the Graduate Honor System.

8 Special Needs

- Reasonable accommodations are available for students who have documentation of a disability from a qualified professional. Students should work through Services for Students with Disabilities (SSD) in 152 Henderson Hall. Any student with accommodations through the SSD Office should contact the instructor during the first two weeks of the semester.
- If participation in some part of this class conflicts with your observation of specific religious holidays during the semester, please contact the instructor during the first two weeks of class to make alternative arrangements.
- If you miss class due to illness, especially in the case of an exam or some deadline, see a professional in Schiffert Health Center. If deemed appropriate, documentation of your illness will be sent to the Dean's Office for distribution to the instruction.
- If you experience a personal or family emergency that necessitates missing class, contact the Dean of Students at 231-3787 or see them in 152 Henderson Hall.

9 Tentative Schedule

Week	Date	Class	Topic	Homework
1	23 Aug	X	(Online) Class Intro	
	25 Aug	X	(Online) MSP430 Microcontroller	
2	30 Aug	C	MSP430 Software Toolflow	
	1 Sep	C	MSP430 Hardware Toolflow	H1
3	6 Sep	C	MSP430 Perf Measurement	
	8 Sep	C	MSP430 Mem Mapped Interface	H2
4	13 Sep	C	Hardware/Software Communication	
	15 Sep	C	MSP430 Hardware Accelerator	H3
5	20 Sep	C	Inverted Lecture	
	22 Sep	C	Midterm I	
6	27 Sep	C	FPGA-SoC	
	29 Sep	C	FPGA-SoC Software Tool Flow	H4
7	4 Oct	C	FSMD in Verilog	
	6 Oct	X		H5
8	11 Oct	C	FPGA-SoC Software Tool Flow	
	13 Oct	C	FPGA-SoC Software Tool Flow	H6
9	18 Oct	C	HW/SW Synchronization	
	20 Oct	C	Inverted Lecture	
10	25 Oct	C	Midterm II	
	27 Oct	C	On-Chip Bus	H7
11	1 Nov	C	On Chip Bus II, Avalon MM	
	3 Nov	C	Microprogrammed Design	H8
12	8 Nov	C	Microprogrammed Example	
	10 Nov	X		Challenge
13	15 Nov	C	TBD	
	17 Nov	C	Codesign Q&A	
	24 Nov	X	*Thanksgiving Holiday*	
	26 Nov	X	*Thanksgiving Holiday*	
14	29 Nov	C	Performance Tuning	
	1 Dec	C	Performance Tuning	
15	6 Dec	C	Codesign Results	
	8 Dec	X	*Reading Day*	

C = class will meet. X = class will not meet.