ECE 4514: Digital Design II – Spring 2019 – CRN 13112

Version 5/2/2019 3:34 PM

General

- Class Section Meeting Times
  - Section: CRN 13112
  - Time: Tuesday and Thursday 5:00PM-6: 15 PM
  - Venue: Goodwin 145
- Instructor
  - Prof. P. Schaumont
    Durham Hall 337
    540-231-3553
    E-mail: schaum@vt.edu
    WWW: `http://rijndael.ece.vt.edu/schaum`
- TA:
  - Tarun Kathuria
    E-mail: tarun91@vt.edu
- Office Hours Instructor (Durham 337)
  - Tuesday 2 PM - 4 PM
  - Thursday 2 PM - 4 PM
- Office Hours TA (CEL)
  - TBD
- Class Webpage:
  - https://canvas.vt.edu/courses/83495
  - https://piazza.com/class/jqelkk8ma0q38o

Description

Advanced digital design techniques for developing complex digital circuits. Emphasis on system-level concepts and high-level design representations while meeting design constraints such as performance, power, and area. Hardware description language simulation and synthesis tools are used to design a series of increasingly complex digital systems.

Formal Objectives

Having completed this course, you will be able to

- Apply advanced design strategies that include testing and debugging techniques;
- Meet specified design constraints, such as performance, power, and area, using contemporary techniques;
- Use multiple clocks and asynchronous system techniques for high-speed data transfer;
- Prototype complex digital systems that meet specific design constraints;
- Compare and contrast the relative capabilities of various contemporary digital hardware technologies.

Prerequisites

You need to have passed ECE 3544 with a grade of C- or better to take ECE 4514. The course assumes that you already know the basics of Verilog programming, as is covered in ECE 3544 and ECE 2504.

Equipment, Design Software and Textbook

- You will be making use of the DE1-SoC Altera Design Kit by TerASIC (http://de1-soc.terasic.com). The DE1-SoC is a high-performance FPGA board equipped with a Cyclone V Series device. You will receive a loaner board, free-of-charge, for the duration of the course. You will have to return the board to the department at the end of the semester. If you fail to return the kit, you will receive an incomplete (I) grade. Instructions regarding distribution and collection of these kits will be given in class.
- You will need the following design software will be required. The installation instructions will appear on the course website.
    - Altera Quartus Prime Lite Edition version 17.0 or better
    - Altera Modelsim version 10.5b or better (included in Quartus Prime Lite)
    - Verilator 4.008 or better
- You do not have to buy a textbook. I will post a series of references and reading assignments of online material. The material includes online textbooks, articles, data-sheets and manuals.

Assignments

- There will be **ten homework** over the semester.
    - Each assignment must be solved in one (or, exceptionally, two) weeks. The exact turn-in date for each assignment is announced for each assignment.
    - Assignments will be distributed and collected through GitHub Classroom. The use of GitHub Classroom will be clarified during the lecture.
    - There is no late policy in this course. Late homework gets a zero (0) grade.
    - You are responsible for keeping the class equipment (including the FPGA board, the laptop/workstation, and the design software) in good working condition. Late assignments because of technical issues are not accepted.
    - The last two homework (HW9 and HW10) will be open-ended and structured as a design project.
- Unless explicitly stated otherwise, all assignments are individual assignments and must be completed independently by the students.
- You can use the Piazza Forum listed on the front page of the syllabus to ask questions and conduct public discussions related to the assignments. I strongly encourage you to use the forum.
    - If you're in doubt if a certain question or answer would violate the Honor Code, check with the instructor first (schaum@vt.edu). By default, I encourage you to discuss design problems publicly.

Grading

Semester grades will be based on the following weights.

- Homework Assignments (10 in total): 64% of the points
- Exam I: 12% of the points
- Exam II: 12% of the points
- Exam III: 12% of the points

The exam dates are listed on the tentative schedule further in this syllabus. An exam may be exceptionally rescheduled for an individual student provided a valid reason has been approved by the instructor at least one week before the exam date.

Grading errors on assignments or exams can be appealed within one week after the graded assignment was returned to the student. Appeals must be made to the instructor.

Note the heavy weight of Homework in your course grade. ECE 4514 is a Design Technical Elective, which means that the practical experience you gain from this course is an important outcome. The 10 Homework may carry different weights, with the later Homework counting for a larger portion of the overall Homework grade.

Honor Code Policy

Students enrolled in this course are responsible for abiding by the Honor Code. A student who has doubts about how the Honor Code applies to any assignment is responsible for obtaining specific guidance from the course instructor before submitting the assignment for evaluation. Ignorance of the rules does not exclude any member of the University community from the requirements and expectations of the Honor Code. For additional information about the Honor Code, please visit http://www.honorsystem.vt.edu.

The bottom line is this. The Honor Code is a serious matter. Don't play games you cannot win.

Here's a practical rule of thumb: *For individual assignments, you cannot receive or give out Verilog code that you or another student wrote.* This applies to any possible form of receiving and giving source code, such as email attachments or screenshots, IM with snippets of code, looking at someone else's screen or showing your screen, reading out loud your file line by line within earshot of your peers, …

Special Needs

- Reasonable accommodations are available for students who have documentation of a disability from a qualified professional. Students should work through Services for Students with Disabilities (SSD) in 152 Henderson Hall. Any student with accommodations through the SSD Office should contact the instructor during the first two weeks of the semester.
- If participation in some part of this class conflicts with your observation of specific religious holidays during the semester, please contact the instructor during the first two weeks of class to make alternative arrangements.
- If you miss class due to illness, especially in the case of an exam or some deadline, see a professional in Schiffert Health Center. If deemed appropriate,

documentation of your illness will be sent to the Dean's Office for distribution to the instruction.

- If you experience a personal or family emergency that necessitates missing class, contact the Dean of Students at 231-3787 or see them in 152 Henderson Hall.

Tentative Schedule

Wk	Date	Lec	Methods	Tools	HW
1	01/22/19		Digital Logic		
	01/24/19			GitHub	HW1
2	01/29/19		FSM		
	01/31/19			HDL Simulators	HW2
3	02/05/19		FSMD		
	02/07/19			HDL Simulators	HW3
4	02/12/19		HW2/3 Review		
	02/14/19			Digital Audio	
5	02/19/19			CORDIC	HW4
	02/21/19		Performance		
6	02/26/19			Review	
	02/28/19		Exam I		
7	03/05/19		FPGA vs ASIC Tech		HW5
	03/07/19			Signal-Tap	
8	03/19/19		Area-Time Tradeoff		
	03/21/19			Area/Time Tradeoff	HW6
9	03/26/19 *		Memory Synthesis		
	03/28/19 *			Timing Simulation	HW7
10	04/02/19		Pipelining and Retiming		
	04/04/19			Unfolding	HW8
11	04/09/19		Review		
	04/11/19			Exam II	
12	04/16/19		QSYS		HW9
	04/18/19			Multi-clock Design	
13	04/23/19		Keyboard Interfacing		
	04/25/19			Divider	HW10
14	04/30/19		Chip Biometrics		
	05/02/19			Review	
15	05/07/19		Project Discussion		
	05/09/19		Reading Day		
	05/11/19		Exam III		

- Lecture topics are tentative. This schedule may be adjusted through the semester.
- Exam days are fixed.
- * indicates instructor on travel. Lectures will be online. Exams will be in-class.

- HW indicates the hand-out date. The turn-in date will be one week after hand-out unless announced otherwise.