VERILATOR

Your Big 4th Simulator: 2019 Intro & Roadmap

Verilator

SystemVerilog
RTL design

```
module ff
  (input clk, d,
   output logic q);
  always_ff @(posedge clk)
   q <= d;
endmodule
```

Simulation
Executable

- Super Fast
- License Free
- Runs Anywhere
- Buildable into apps
- 100% C++ code

Lint

XML

Users' tools

Verilator is one of the “Big 4” Simulators

- RISC-V vendor:

  “We support the **big 4** simulators… VCS, Modelsim, Cadence, **Verilator**”

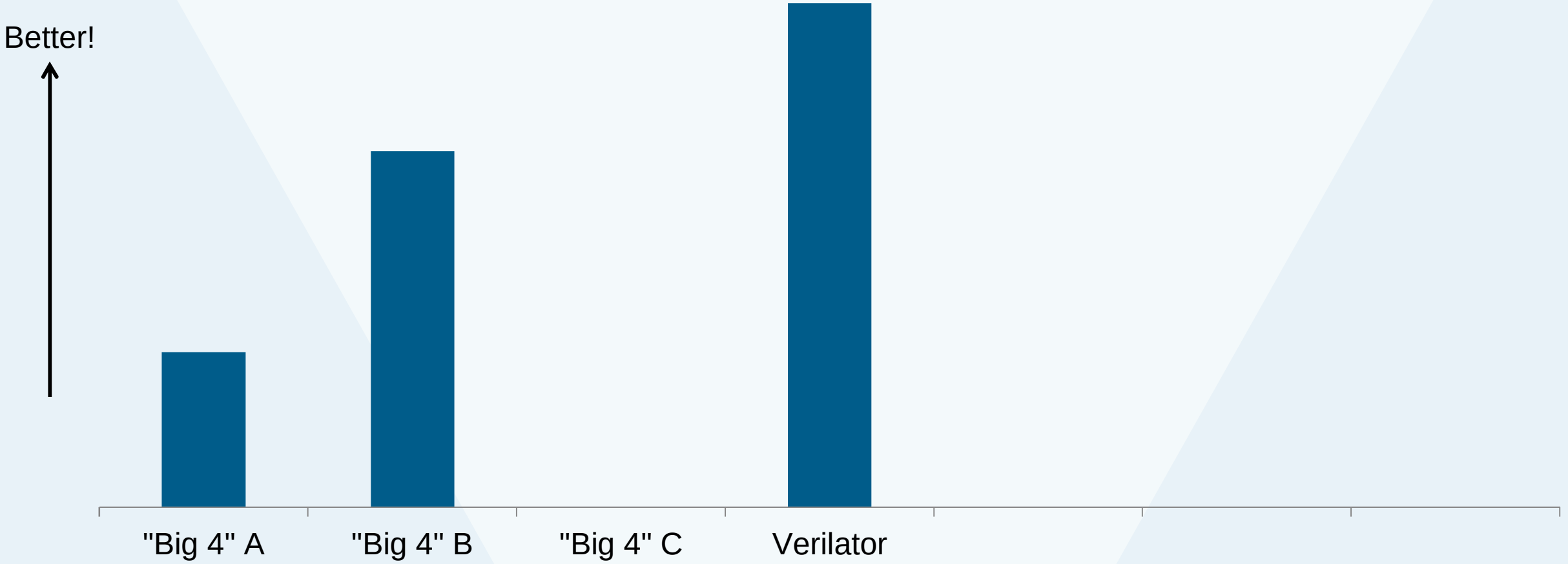
- ARM CPU IP:

```
reg clk_en_lat /*verilator clock_enable*/;
```

- Supported by most open-source HW IP

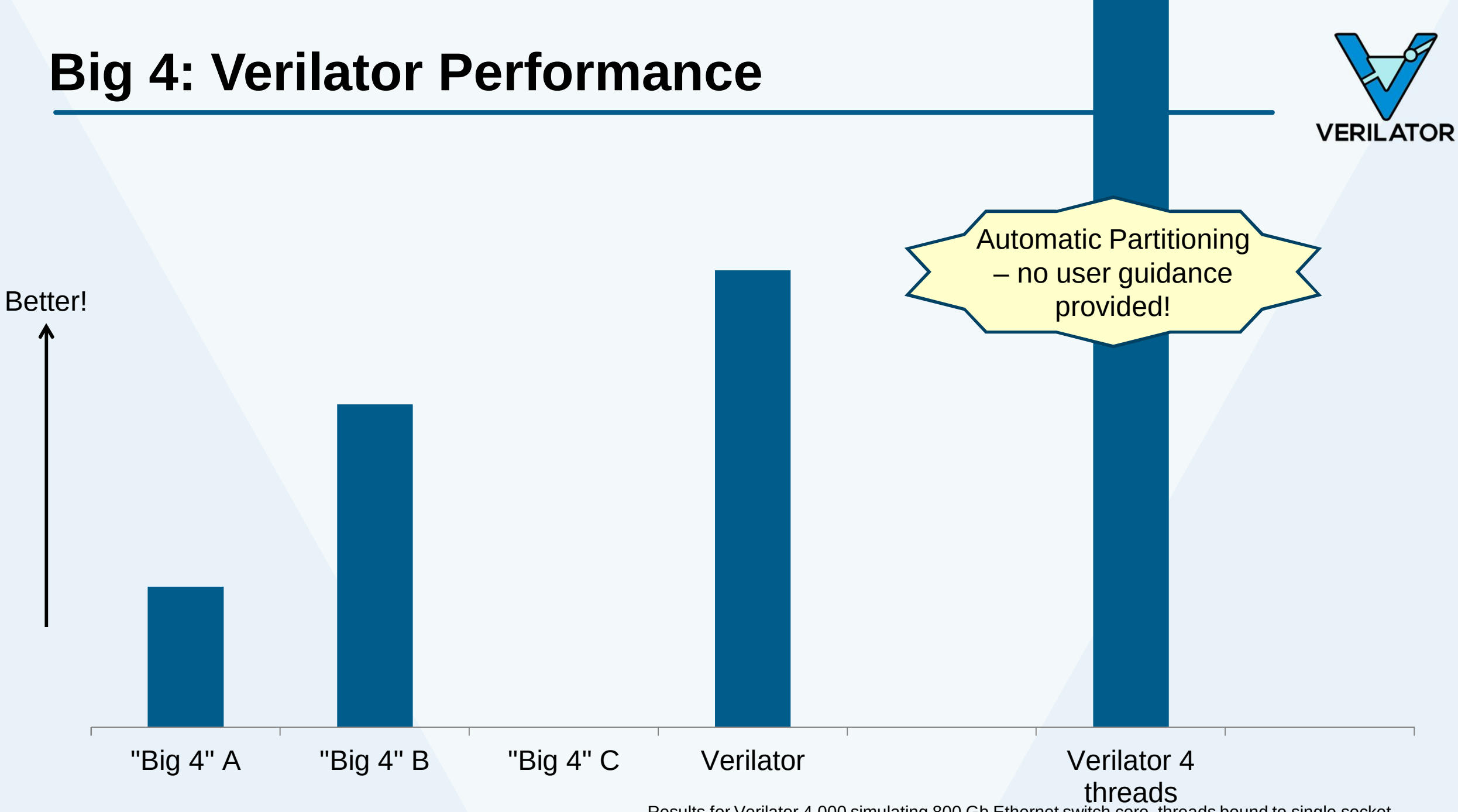
- Internal use in major CPU & SoC design centers (some for 20 years)

Big 4: Verilator Performance



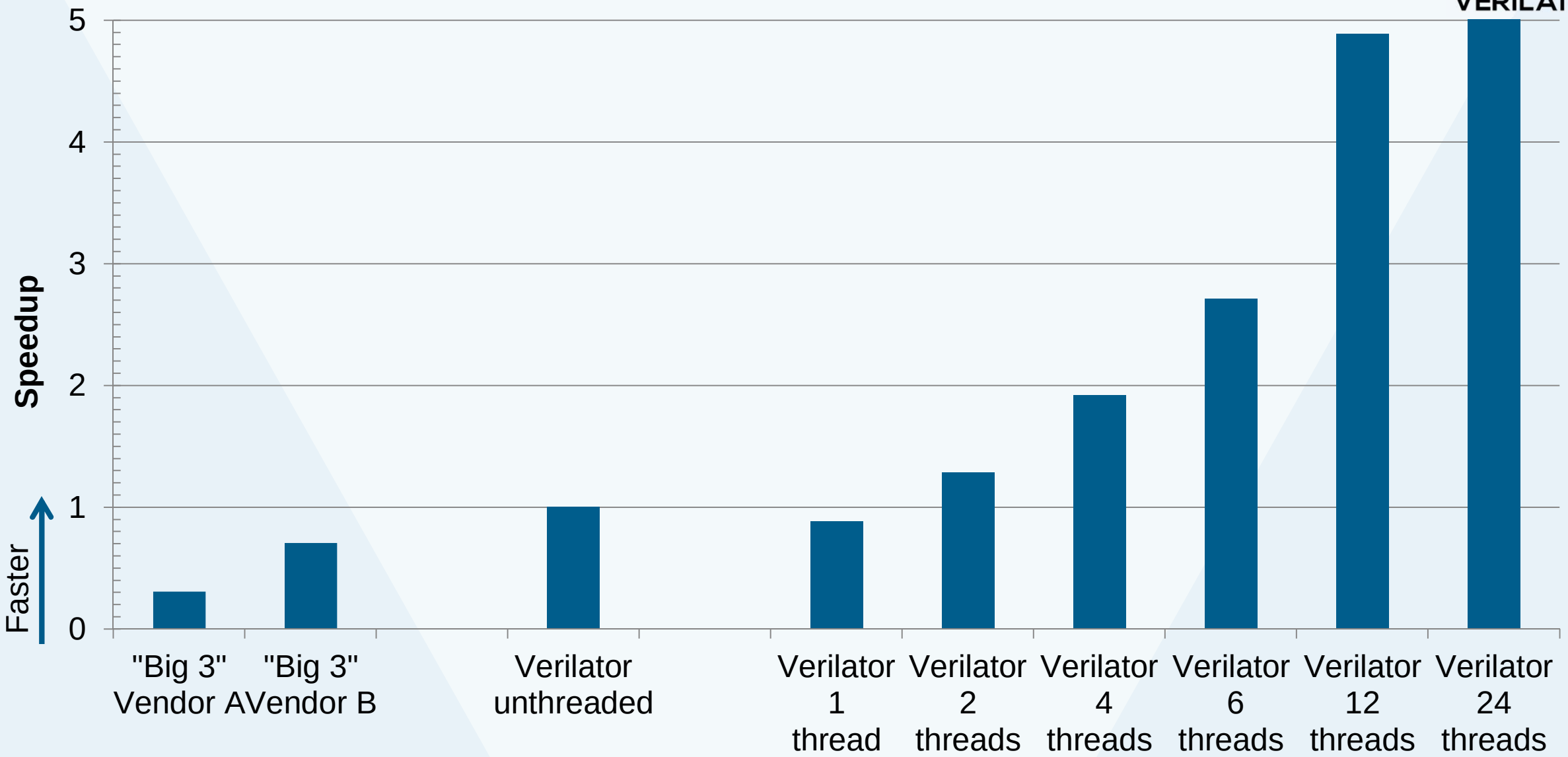
Results for Verilator 4.000 simulating 800 Gb Ethernet switch core, threads bound to single socket

Big 4: Verilator Performance



Results for Verilator 4.000 simulating 800 Gb Ethernet switch core, threads bound to single socket

Verilator Multithreaded Performance



Results for Verilator 4.000 simulating 800 Gb Ethernet switch core, threads bound to single socket

Many Contributors… Thanks to all

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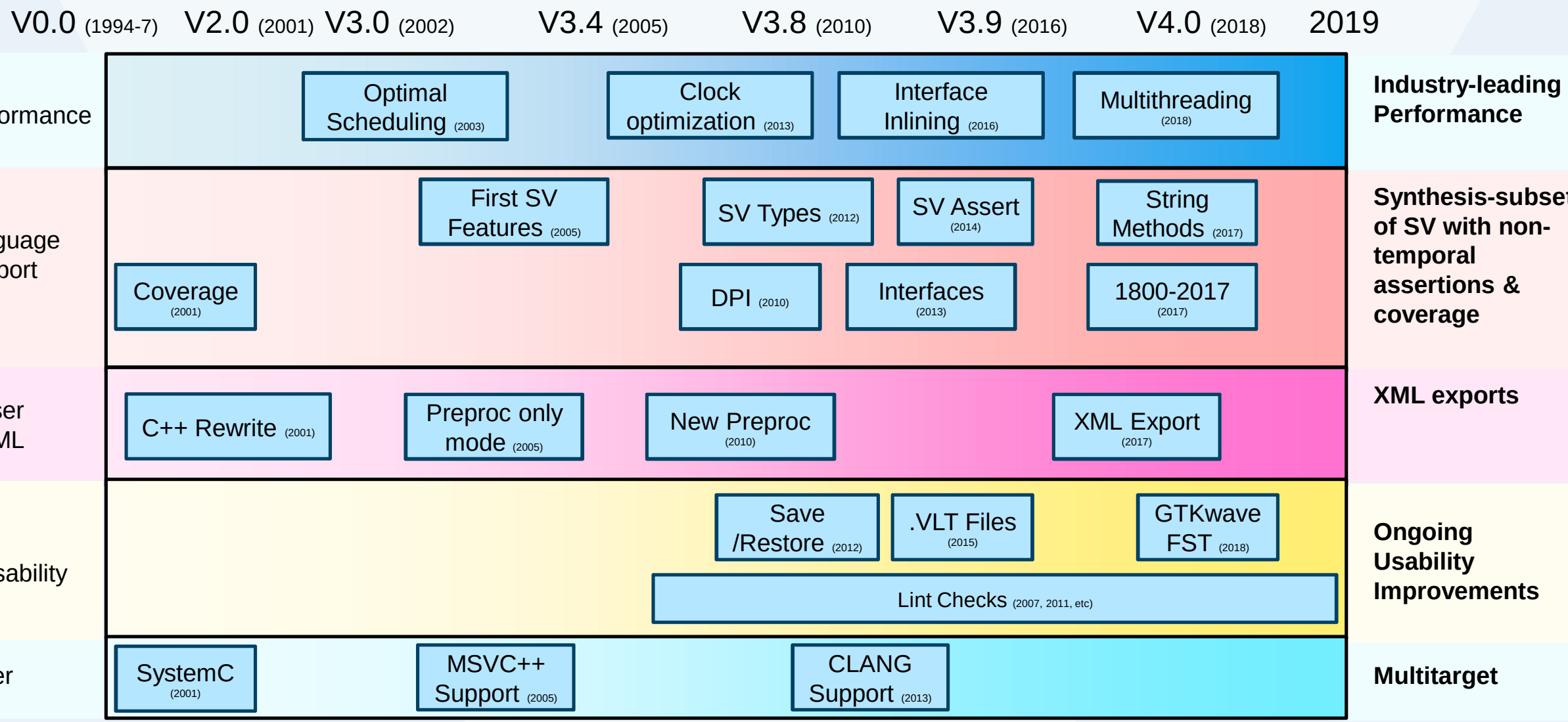
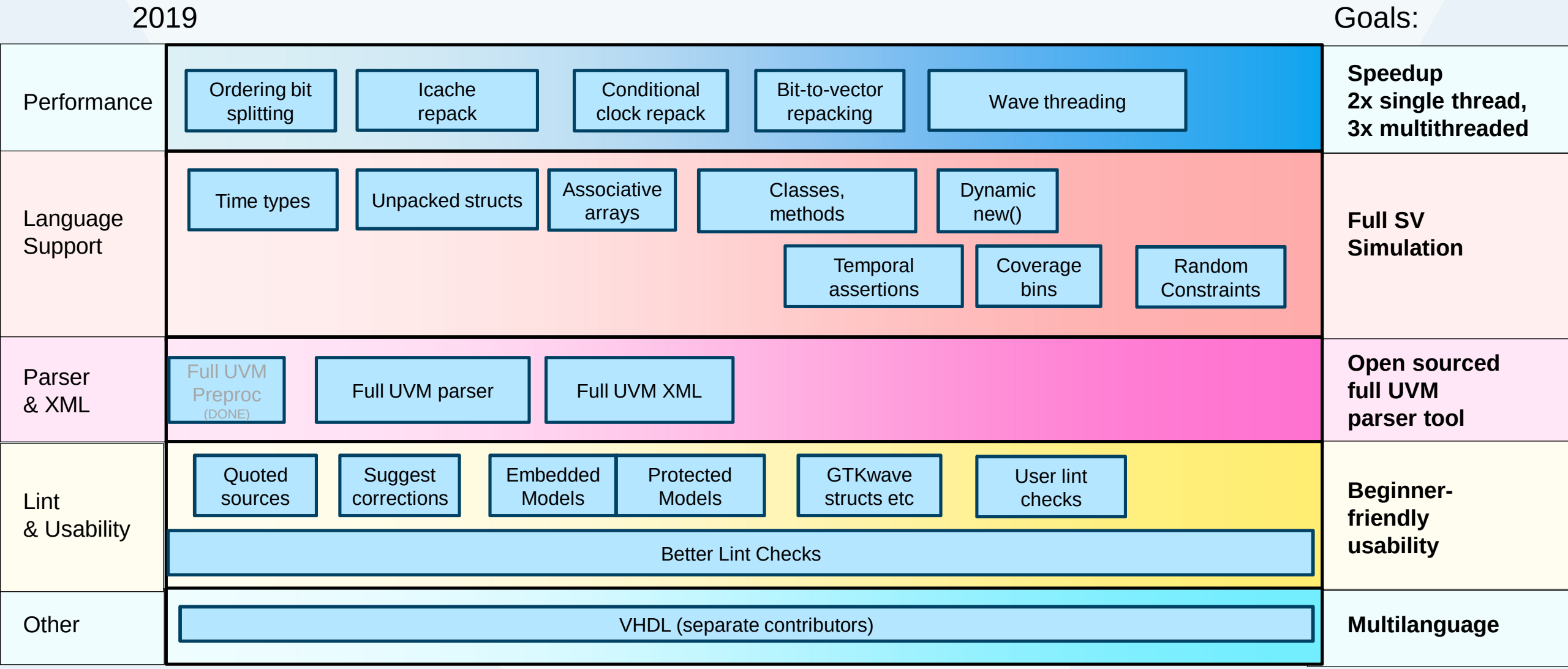
Thanks to them, and any we've missed including, and those who whished to remain anonymous.

Historical Roadmap



Future Roadmap



Adopt Verilator as Your Big-4th

Supported

- Continual improvements
- Growing support network for 25+ years

Open Source Helps You

- Easy to run on laptops or SW developer machines
- Get bug fixes in minutes rather than months
- Spend simulator license $$ instead on computes
- Greatly aid commercial license negotiation

Keep your Commercial Simulators

- SystemVerilog UVM tests, analog models, gate SDF, etc.

Value of Open Source is the Community!

Provide Verilator support in your IP

Contribute to Verilator Forums and Bug Reporting (http://verilator.org)

Contribute a patch or Engineering resources

Advocate!

Also at Veripool: Verilog-Mode for Emacs

- Thousands of users, including most IP houses
- Fewer lines of code to edit means fewer bugs
- Indents code correctly, too
- Not a preprocessor,
  code is always “valid” Verilog
- ★Automatically injectable
  into older code.

```
  …
/*AUTOLOGIC*/

a a (/*AUTOINST*/);
GNU Emacs   (Verilog-Mode)
```

```
/*AUTOLOGIC*/
// Beginning of autos
logic [1:0] bus; // From a,b
logic       y;   // From b
mytype_t    z;   // From a
// End of automatics

a a (/*AUTOINST*/
     // Outputs
     .bus   (bus[0]),
     .z     (z));
GNU Emacs   (Verilog-Mode)
```

Resources

- Verilator and open source design tools at http://www.veripool.org
  - Downloads
  - Bug Reporting
  - User Forums
  - News (add yourself as a watcher to see releases)
  - Presentations at http://www.veripool.org/papers/