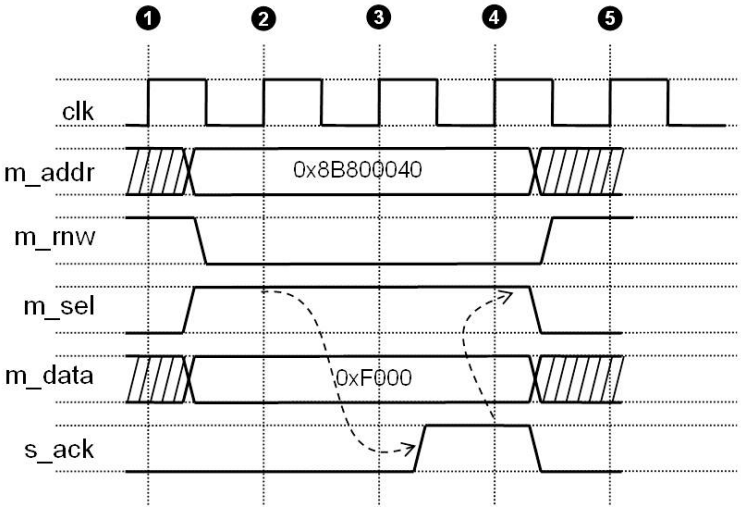
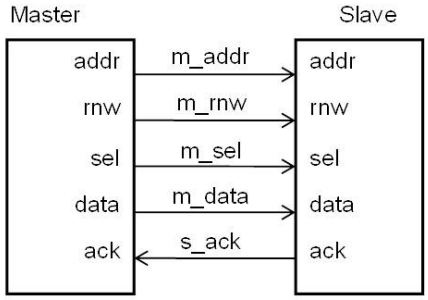
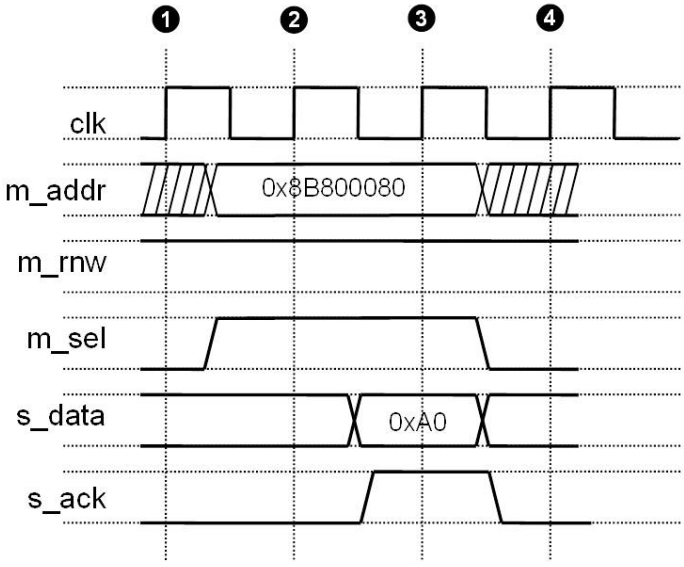
ECE 4530 Fall 2019: Handout Lecture 11

Generic-Bus Write Operation





Generic-Bus Read Operation



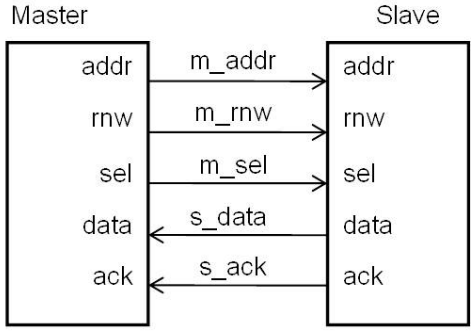


Table 1: Signals on the generic bus

Signal name	Meaning
clk	Clock signal. All other bus signals are references to the upgoing clock edge.
m_addr	Master address bus.
m_data	Data bus from master to slave (write operation).
s_data	Data bus from slave to master (read operation).
m_rnw	Read-not-Write. Control line to distinguish read from write operations.
m_sel	Master select signal, indicates that this master takes control of the bus.
s_ack	Slave acknowledge signal, indicates transfer completion.
m_addr_valid	Used in place of m_sel in split-transfers.
s_addr_ack	Used for the address in place of s_ack in split-transfers.
s_wr_ack	Used for the write-data in place of s_ack in split-transfers.
s_rd_ack	Used for the read-data in place of s_ack in split-transfers.
m_burst	Indicates the burst type of the current transfer.
m_lock	Indicates that the bus is locked for the currrent transfer.
m_req	Requests bus access to the bus arbiter.
m_grant	Indicates bus access is granted.

Generic-Bus Arbitration